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A FUNCTIONAL DESCRIPTION OF THE GEOPHYSICAL DATA ACQUISITION SYSTEM

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13. ABSTRACT (Maximum 200 words)

The Geophysical Data Acquisition System, GDAS, is a modified and updated version of the Standalone Data Acquisition, SDAS, (Von Glahn, 1980). This report parallels Von Glahn's, taking freely from it and maintaining its format while emphasizing the changes, modifications, and updates made during the decade. Functional descriptions of the subsystems are expanded where needed and full descriptions of the peripheral interfaces including figures depicting jumper configuration for operation within the GDAS, have been added.

The purpose of the GDAS has remained the same, that is, a portable computer controlled data acquisition system, with new emphasis on portability and environmental operation. Modifications to the frontend analog section, which underwent a total change, include the flexibility of a remote preamplifier system, and a current mode calibration system. The use of various geophysical sensors was also considered in this redesign.

The software section of this report presents a brief description of the CAD (Computer Aided Design) and calibration programs. A parallel report covers the software engineering, and data reduction software developed GDAS (Center, 1989).

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1.0 INTRODUCTION

1.1 REPORT OVERVIEW

This report describes the modification and update of the AFGL Standalone Data Acquisition System (SDAS) (Von Glahn, 1980). It details the evolution of SDAS into its present configuration, now known as the Geophysical Data Acquisition System (GDAS). Although GDAS retains much commonality with its predecessor, its performance has improved significantly and it has greatly expanded capabilities. Our report supplements Von Glahn's earlier publication from which we have extracted substantial information, drawings and schematics presently relevant to, and valid for GDAS.

During the past decade increasingly complex military activities, siting criteria and facility response to seismo/acoustic energy necessitated development of state-of-the-art techniques and equipment having increased accuracy, reliability, and vastly expanded data collection/analysis capabilities. GDAS represents a series of redesigns and modifications directed toward improved operational capabilities, greater flexibility, minimization of natural and induced noise effects, and developing and implementing more sophisticated software techniques. In addition, Weston Observatory has continuously upgraded the overall system so that it is much more versatile and now can be used for on-line definition and analysis of many types of geophysical data.

GDAS has no standard configuration which encompasses all field applications. It is designed with a great deal of inherent flexibility which permits tailoring for specific requirements with minimal effort and change. Each deployment considers program objectives, type and number of sensors, length of data cables, storage devices, etc. that dictate how the system will be integrated. In addition to specialized operational assets, ambient environmental factors at each site are considered.

Customized fiberglass shipping cases are used for transporting the GDAS. The system console and other non rack-mounted equipment fit into individual foam padded shipping containers. Other components are placed in shock-mounted equipment racks housed in fiberglass enclosures, except for the junction box, which is packed separately. Extra room has been designed into the racks to safely transport delicate test equipment (oscilloscopes/digital multimeters, etc.) as necessary to set-up, calibrate, test and maintain the GDAS.

1.2 REPORT ORGANIZATION

This report primarily concerns the hardware aspects of GDAS. It details changes made to the equipment since the last report; describes why the changes were necessary; and documents resultant improvements and methods of operation. Individual chapters contain detailed schematics and specifications including a functional description of modified subsystems. Relevant SDAS material and procedures which have not changed are included verbatim in our current report. A second report (Center, 1989) concerns itself with software developed under the program with emphasis on the most recent applications. It describes the operational aspects of programming the GDAS for field data collection, and also details various procedures for reducing and analyzing data.

2.0 SYSTEM OVERVIEW

2.1 PURPOSE OF SYSTEM

The Geophysical Data Acquisition System is a portable digital data recording system designed specifically to collect and analyze geophysical data in the field. GDAS accepts analog electrical signals from sensors, conditions the signals, converts them to digital form and records the resultant information on a mass storage device.

2.2 SYSTEM ORGANIZATION

GDAS consists of three groups of components; a sensor array, junction box and a recording set. (see Figure 1)

The sensor array allows for deployment of similar sensing units, or of a combination of different types (seismic, acoustic, pressure, displacement, temperature, force, etc.). They can be either active or passive, and can be positioned hundreds of feet from each other and other operational components.

The junction box, located at a convenient central point, collects signals from individual sensors, conditions them and then routes them to the recording set. The junction box also supplies power to the active sensors, and conditions and distributes the calibration signal sent to it by the recording set. A sound powered telephone can be connected to the junction box to communicate with the recording set during set up, calibration, or as needed to coordinate operations.

The third group of components, the recording set, comprises a major portion of the GDAS and includes the computer. This ensemble is preferably located within a controlled room or other enclosure, but under certain circumstances it can be positioned at less sheltered field sites when it is possible to operate the equipment within normal environmental parameters.

Signals are relayed from the junction box over multi-paired cables to the switch box (a series of terminal boards) that can simultaneously receive input from as many as three junction boxes. The terminal boards can be set up to select which sixteen channels of the available thirty are processed. The selected channels are routed to the signal conditioner subsystem for amplification, filtering and anti-aliasing filtering. After conditioning, the analog signals are fed to an A/D converter for conversion to digital format. The A/D converter works in conjunction with its interface and is under control of the computer, both of which are located in the controller subsystems. The digital data is then routed to one of the GDAS mass storage devices.

The controller is a micro-computer running under programs stored in one of the mass storage devices associated with GDAS. It is the heart of the system, controlling all aspects of the data collection and reduction.

An interface subsystem houses the GDAS calendar clock, which provides time, the Julian date, and a time variable pulse train used as a sampling clock. Additional circuitry required to buffer the time and date information to the computer are housed in this subsystem. The time and date information are added to the data stream by the computer for recording on the selected mass storage device. Also included within the interface subsystem is a pair of level converting cards used to interface the digital magnetic tape recorder read, write, and control information with the computer for proper operation.

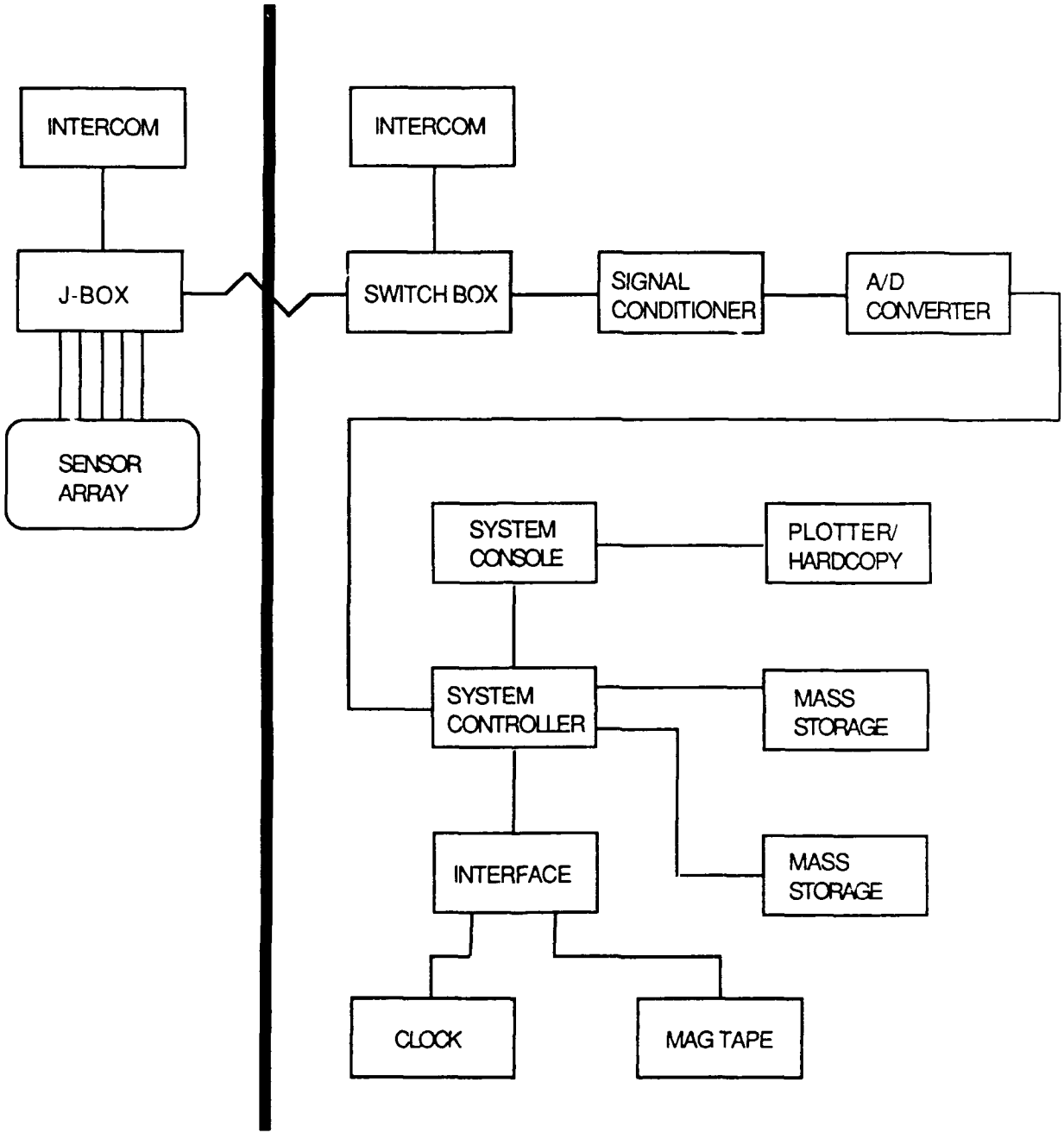


FIGURE 1: GDAS BLOCK DIAGRAM

The system console connected to the controller allows the operator to communicate with the computer. Graphics output (plots) or listings (printouts) can either be displayed on the console or on a plotter or hard copy device connected to, and run from the system console. Software control of both is also possible.

GDAS has been designed and packaged so that it can be easily transported and installed at remote locations accessible by a small, van type vehicle. However, there are some constraints on how and where it can be used. The junction box, which is completely sealed from the weather, must have a reliable 110 VAC, 60 Hz power source available. The box must be positioned within a few thousand feet of the recording set; depending upon requirement and/or the length of the interconnecting cables. Additionally, the recording site, which also requires a 110 VAC, 60 Hz power source, must provide temperature/humidity control commensurate with the operation of standard commercial electronics.

2.3 SYSTEM SPECIFICATIONS

Specifications for the overall system are given in Table 1 of this section. Detailed specifications for each subsystem are listed in individual sections which describe each function.

TABLE 1 SYSTEM SPECIFICATIONS

Number of channels	up to 16
Power requirement	115V AC 60 cy ± 5% 15 Amp service Actual current requirement varies with configuration
Operating temperature	
Junction box	-20° to +75° C
Major system Electronic	+15° to +32° C
Analog section noise	10 µV pp - DC-200hz RTI
Digital noise	± 2 LSB
Signal capability	± 10 Volts
Analog gain	>0< $2x10^5$ DC coupled Gain may be increased with AC coupling, reduced reliability
Digital Resolution	14 bit plus sign
Frequency response	
Analog	DC-1000 hz
Digital Sample rate	Maximum samples/sec varies with program variation and recording device: Not less than 50 SPS nor greater than 250 SPS

3.0 SENSORS/TRANSDUCERS

3.1 CHAPTER OVERVIEW

Most of the research supported by GDAS has primarily involved two types of transducers, seismic and pressure. Several other kinds of transducers (deflection, tilt, wind speed, etc.) have been incorporated into the overall system in response to special requirements, but, for the sake of brevity, we will only detail the first two mentioned. All sensors are similarly wired, see Figure 2 for connector wiring.

3.2 SEISMIC TRANSDUCERS

Described in the following sub-paragraphs are two seismometers used with GDAS. The system is not restricted to these two and any properly wired seismometer could conceivably be used.

3.2.1 HS 10-1 SEISMOMETER

One seismometer currently used in conjunction with GDAS is the Geo-Space model HS-10-1B. This unit is an adjustable period very low frequency unit designed primarily for field operations. It incorporates a hum-bucking main coil and a remote calibration coil. The environmental cap has been modified to accept a standard GDAS connector and still remain dust and moisture proof. A cable connecting the seismometer directly to the J-box provides routing for the signal and a means for remote calibration of the unit. The frequency of the seismometer may be adjusted mechanically by the adjusting slug, which requires the removal of the environmental cap. The sensitivity or outp' ' may be calibrated electrically through the use of a separate magnetic shunt and calibrati .i coil operated from the recording set (see manufactures calibration booklet).

3.2.2 HS 10-1 NOMINAL PERFORMANCE

Refer to the response graph of Figure 3 and the specifications of Table 2. The intrinsic voltage sensitivity is given as 1.1 volts/mm/sec with an open circuit damping of 35%. Spring design and mounting provide freedom from spurios modes. Coil windings are hum-bucking. The complete unit, with weather cap, but without leveling legs or input connectors measures 4.38" in diameter by 8.38" in length and weighs 11 lbs.

3.2.3 EV-17 SEISMOMETER

Another seismometer used in the GDAS is the Electro-Tech EV-17. Electro-Tech, a division of Mandrel Industries, is no longer in business. However, a large inventory of these units is on hand and the units have exhibited a unit to unit accuracy and stability in the face of extreme rugged handling.

The vertical unit is a variation of the inclined spring suspension design which requires no clamping. The horizontal unit is a swinging gate design, again, requiring no clamping. Electrical characteristics of the two units are identical. Both units are designed with a moving magnet, requiring care in use near magnetic material.

Field repairs and adjustments requiring some disassembly, can be made to these siesmometers. They may be calibrated by a separate, albeit common wound, calibration coil.

PT**-*-12-10-*

PAIR	COLOR	PIN
1	Red	A
1	Black	B
1	Shield	C
2	White	D
2	Black	E
2	Shield	F
3	Green	G
3	Black	H
3	Shield	J

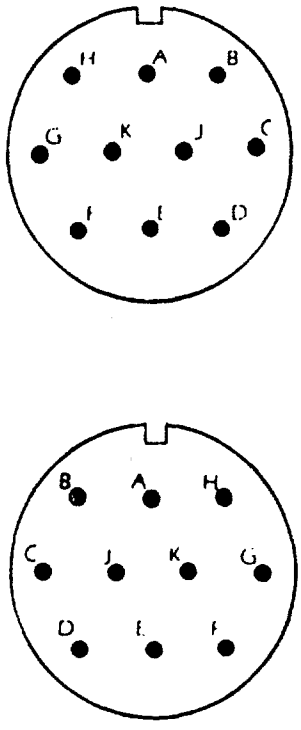


FIGURE 2 CONNECTOR/SENSOR WIRING DESIGNATION

3.2.4 EV-17 NOMINAL PERFORMANCE

A response curve and specifications are given in Figure 4 and Table 3 respectively. The intrinsic voltage sensitivity is .48 volts/mm/sec with an open circuit damping of 33%.

The vertical seismometer measures 4.5" x 8" x 5.5" and weighs 13 lbs. The horizontal unit measures 5.5" x 9" x5.5" and weighs 13.5 lbs.

TABLE 2. GEOSPACE HS 10-1 SPECIFICATIONS

Frequency @ 5-10 MV	1 HZ
Frequency limits @ 1 HZ	.97 to 1.03
DC resistance(DCR) @ 25 C	50,000 ohms
DCR limits @3%	48.500 to 51,500
Number of turns (dual coil, center tapped	50,000
Wire size and type	No.41 AWG
Intrinsic voltage sensitivity (G)	1.1 v/mm/sec
Open circuit damping	35% +/- 10%
Total moving mass	833 gm +/- 1.5%
Motion impedance @ 1 HZ	335,000 ohms
Total impedance @ 1 HZ	385,000 ohms
Calibration coil motor constant	.0326 newtons/amp
Calibration coil sensitivity	1 m.micron/microamp
Calibration coil, number of turns	70
Calibration coil, wire type and size	No. 36 AWG SML
Calibration coil DC resistance	15 ohms +/- 20%

Table 3. ELECTRO-TECH EV-17 SPECIFICATIONS

Frequency	1 Hz
Frequency Accuracy	.025 hz (level indication)
VS 2% tilt	< 2%
DC Resistance	5000 ohms
Intrinsic voltage Sensitivity	.48 v/mm/sec
Open circuit damping	33% ± 5%
Total moving mass	2760 grams
Calibration coil motor constant	10 newtons/amp
Calibration coil sensitivity	100 microns/milliamp
Calibration coil DC resistance	50 ohms

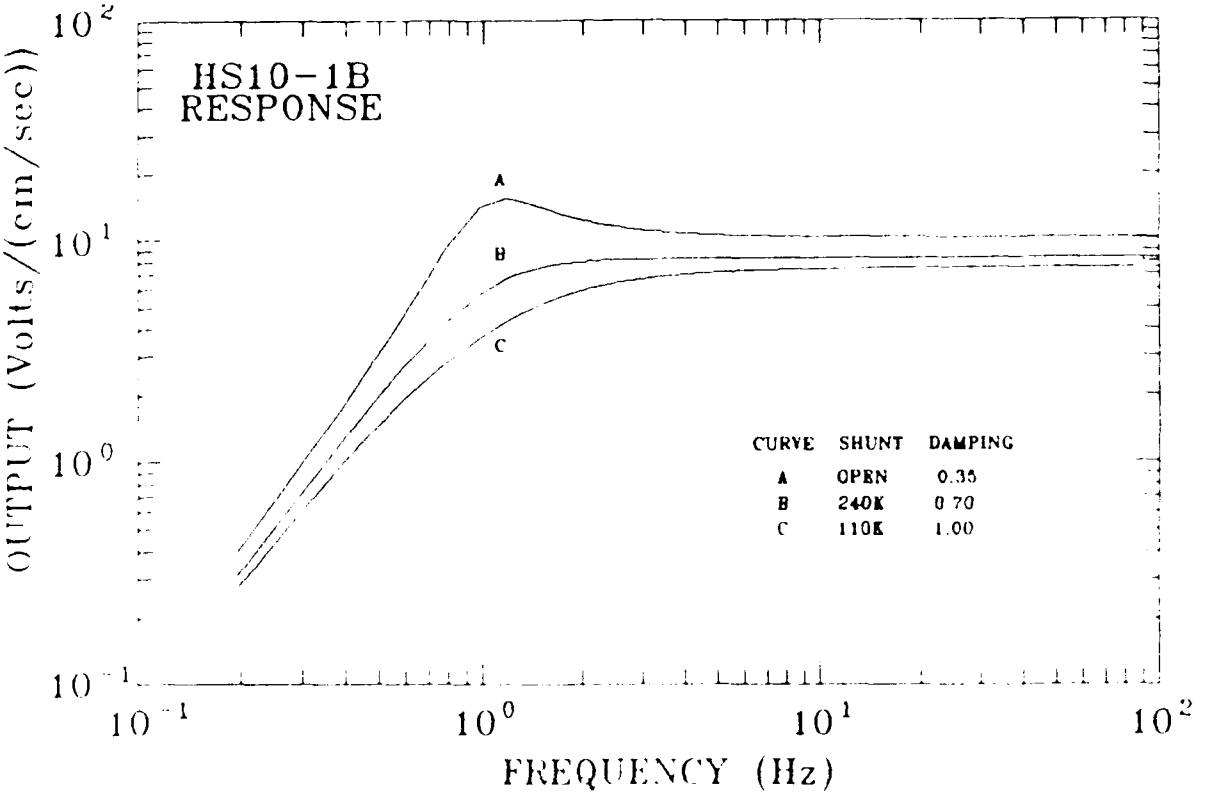


FIGURE 3 HS 10-1 SEISMIC RESPONSE CURVE

3.3 PRESSURE TRANSDUCERS

Two pressure sensors, Micro-Gage, Inc Model P018 (+/- 5.0 PSIG/D) and D.J. Instruments Series MLR (+/- 1.5 PSID) are being used as the sensing element of the transducer. The operating parameters for both sensors are similar, and selection of either unit is based upon specific applications. These sensors are normally housed in the transducer enclosure, but then can be installed without the enclosure as well.

3.3.1 WESTON TRANSDUCER

The transducers, designed and built by Weston Observatory, each contain a sensor, excitation drive, preamp and identifier circuit. All items are packaged in a small (6.16" x 4.13" x 2.68"), extruded aluminum box with removeable end plates, manufactured by Pamona Electronics, model 3742. The box has been made weatherproof and has been painted white in order to help maintain thermal stability in bright sunlight. One end plate has been machined to accommodate a standard GDAS connector which provides power to the transducer and delivers its signal to the system. Also on this plate is a pair of test points and a balance control access port which doubles as a bleeder port. This opening is used to accurately control the bleed rate of the differential transducer to the atmosphere, hence the sensors low frequency response. The opposite end plate is machined to mount the sensor or if required, a connector to accommodate an external sensor.

3.3.2 SENSOR PRE-AMPLIFIER

Performance problems with the original pre-amplifiers led to the design of a quieter, more adaptable unit which subsequently evolved into a preamp that will accommodate any type of bridge sensor. Only the most recent design will be discussed.

Design criteria called for a simple, extremely reliable circuit that minimized thermal drift and which had as few components as possible. Other requirements were for a point-of-load (P.O.L.) regulator to allow better operating characteristics (drift/noise) without regard as to the length of the junction box connecting cable. The new preamp also includes a calibration circuit and various mechanical changes. See Figure 5 for the schematic. The specifications are given in Table 4.

The preamp circuit has a single op-amp split "T" configuration selected because of its use of low resistor values and its subsequent reduction in op-amp current noises. In addition, the "T" configuration further allows for a one resistor change for gain in a differential amplifier. On board balancing, enhanced by the P.O.L. regulator has been utilized. The regulator was specifically selected because of its low noise, wide temperature characteristics. Additional circuitry was designed into the regulator to further reduce the noise.

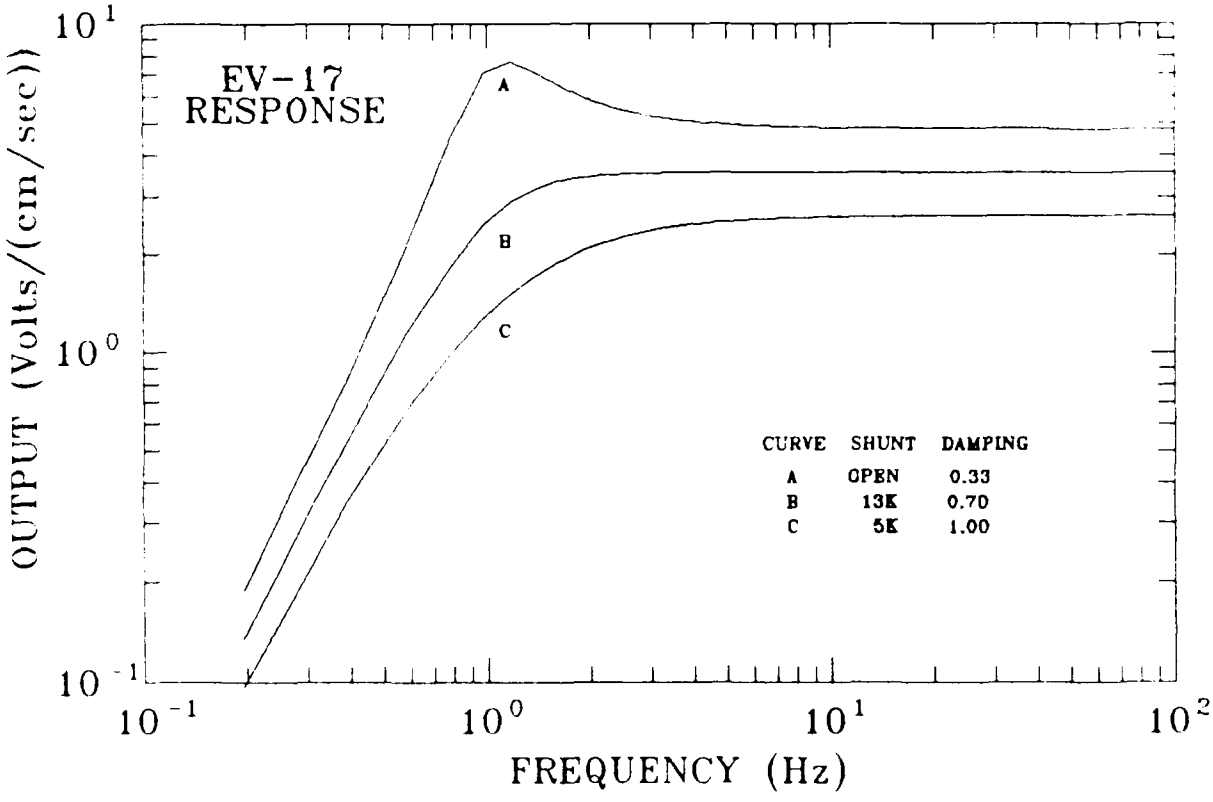


FIGURE 4 EV-17 SEISMIC RESPONSE CURVE

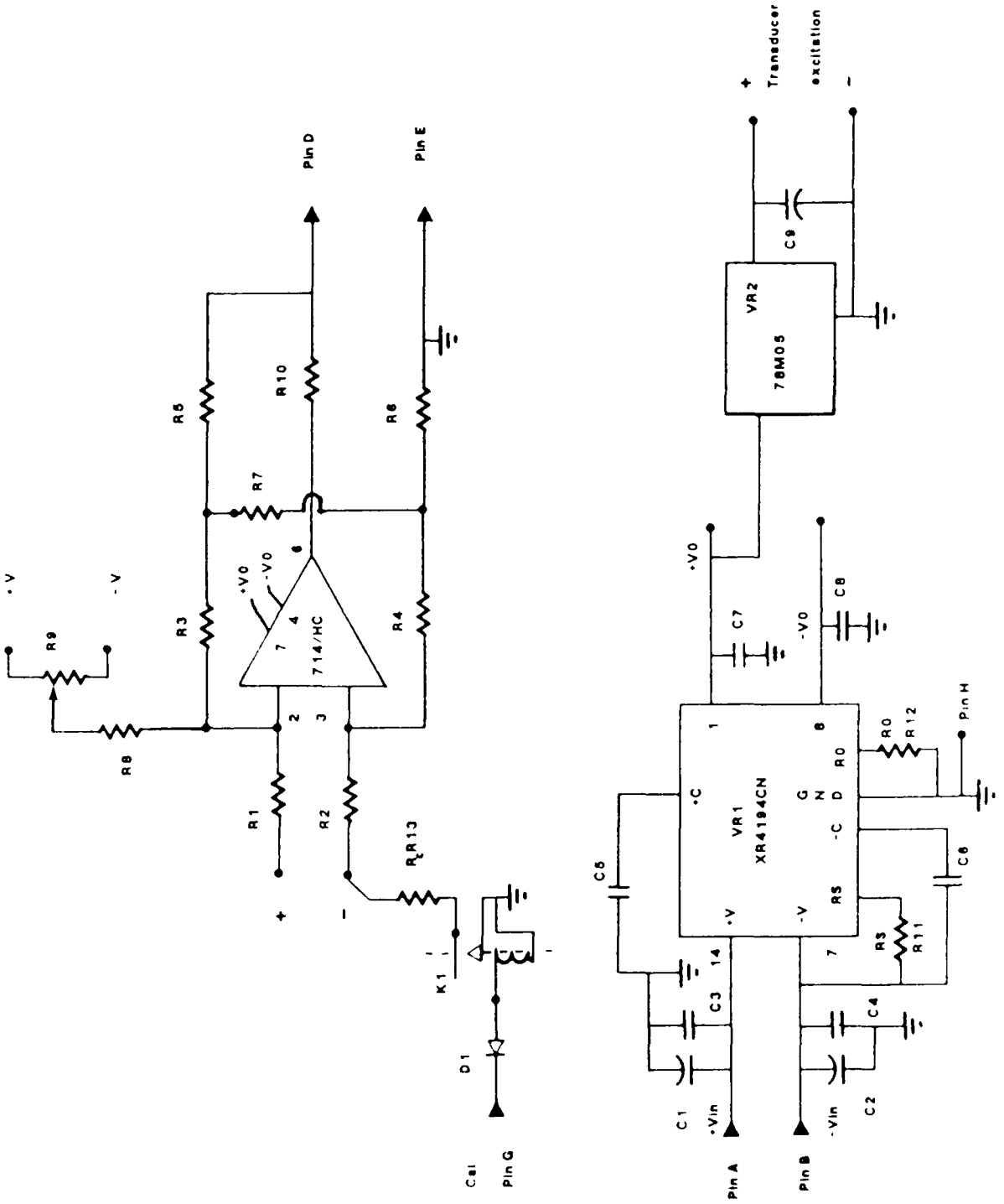


FIGURE 5 PRESSURE TRANSDUCER SCHEMATIC

TABLE 4. PRESSURE TRANSDUCER SPECIFICATIONS

Amplifier type	Psuedo differential
Common mode rejection	> 40 db
Noise (RTI) 0.1 to 100 hz	2.5 μV pp
Frequency response	DC - 10 khz ± 1.0%
Gain range (selectable during Cal)	.5 to 100 V/V
Temperature drift (RTI)	1.5 μV/°C
Sensor Range	
Micro Gage	± 5 PSID
DJ Inst.	± 1.5 PSID
Temperature effect	< 1% FSO / 100°F
Sensitivity	
Micro Gage	± 200 mv FSO
DJ Inst.	± 80 mv FSO
Frequency response	
Micro Gage	> 2 khz
DJ Inst.	2 khz
Transducer calibration	
Sensitivity	± 4.0 V/psi
Frequency response	DC - 1 khz
Calibration level	(-) 0.1 psi

A simple calibration circuit, comprised of a relay and a selected test resistor, was also added to the preamp. When the relay is activated it applies the resistor across one leg of the bridge thereby producing a known offset. While not actually calibrating the sensor it does produce a scale factor offset. A change in this scale factor reflects either an amplifier or sensor change. Required modifications to the calibrator circuit are discussed in later paragraphs.

3.4 TRANSDUCER SERIAL IDENTIFIER

After manufacture of the sensor amplifier, a request for a serial identifier to aid in logging the many and varied types of transducers was acknowledged. Design criteria dictated that it work with and within the transducer package, and that its signal, a digital presentation of the transducer parameters, be impressed on the analog signal and passed on to be recorded by the system. Installation of this circuit causes a minor reduction in differential balance of the amplifier and produces a cumbersome gain equation. The gain is intended to be set during calibration of the sensor- amplifier to produce a normalized transducer output negating this difficulty.

3.4.1 PHYSICAL DESCRIPTION

The serial Identifier is mounted on a 5.60" by 3.875" printed circuit board and is housed inside the transducer box. It is wired to the transducer preamp board to obtain its power and input, and to deliver its output to the preamp by a subtractor routine.

3.4.2 CIRCUIT DESCRIPTION

Refer to Figure 6 for the block diagram. An interrogation input is fed to the pulse width discriminator. If conditions are met, an output enables a clock that in turn feeds a cascaded Johnson counter with 18 descrete outputs. The gating circuit converts these signals to a serial pulse train consisting of a start pulse, 16 information bits, and a stop pulse. The output of the identifier is impressed on the preamp signal by the subtractor input of the op amp.

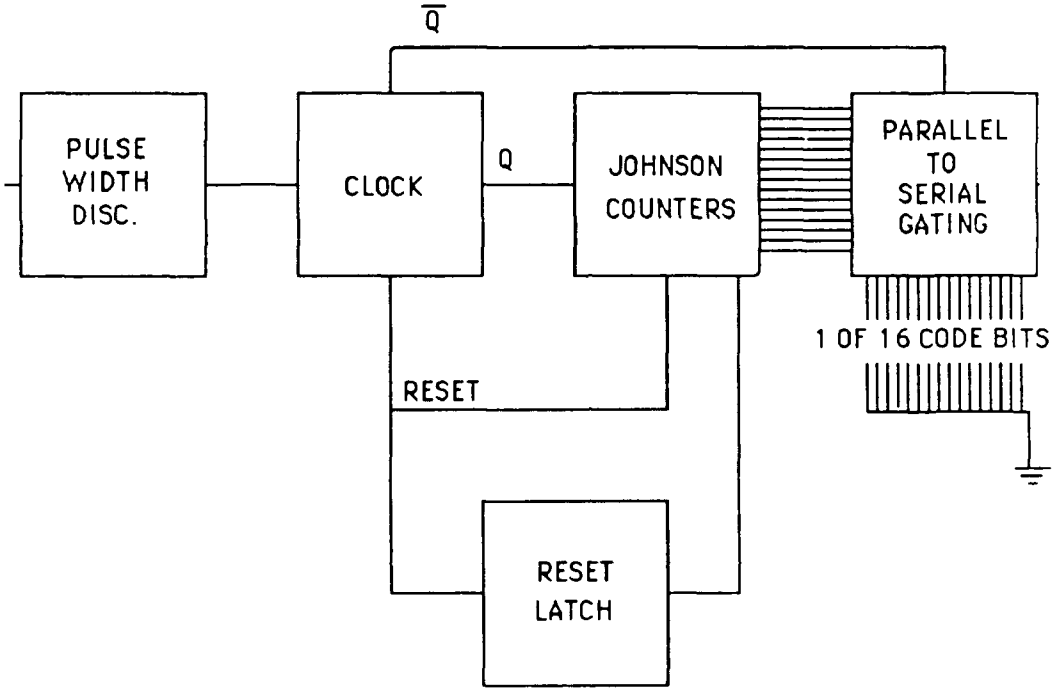


FIGURE 6 SERIAL IDENTIFIER BLOCK DIAGRAM

3.4.3 THEORY OF OPERATION

A complete circuit schematic is shown in Figure 7. The cal pulse from the preamp/line driver, normally a +12V to -12V pulse to drive the cal relay, is also coupled to the circuit. D1 allows only the positive portion through, and R1, R2 divide it to a 5V level for the logic.

IC1A & B and IC2A comprise a pulse width discriminator, forcing the circuit to work only when the input pulse is shorter than 1 ms. IC1 delays the input by 1 ms. Its inversion output, (Q), is NAND'd with the input line. If the cal pulse is still present at the input to the NAND gate, no output results from IC2A. If the input pulse is shorter than 1 ms, a negative pulse (IC2-3) will toggle the R-S latch IC2-C, IC2-D producing ENlo which turns on an astable multivibrator and enables the two cascaded counters IC4 and IC5. (Note: a pulse longer than 1 ms will operate the calibration circuit).

The "Q" output of the MV is sent to the counter which produces a discrete output for each input pulse. The initial output (O0) is on only for the duration of the propagation delay of IC3, (approximately 150 ns) and is thus ignored. IC4 produces eight sequential parallel outputs, O1A through O8A. O9A turns off IC4 which holds its count and when AND'd (IC12B) with the MV output starts IC5 counting on the next positive transition. IC5 then produces

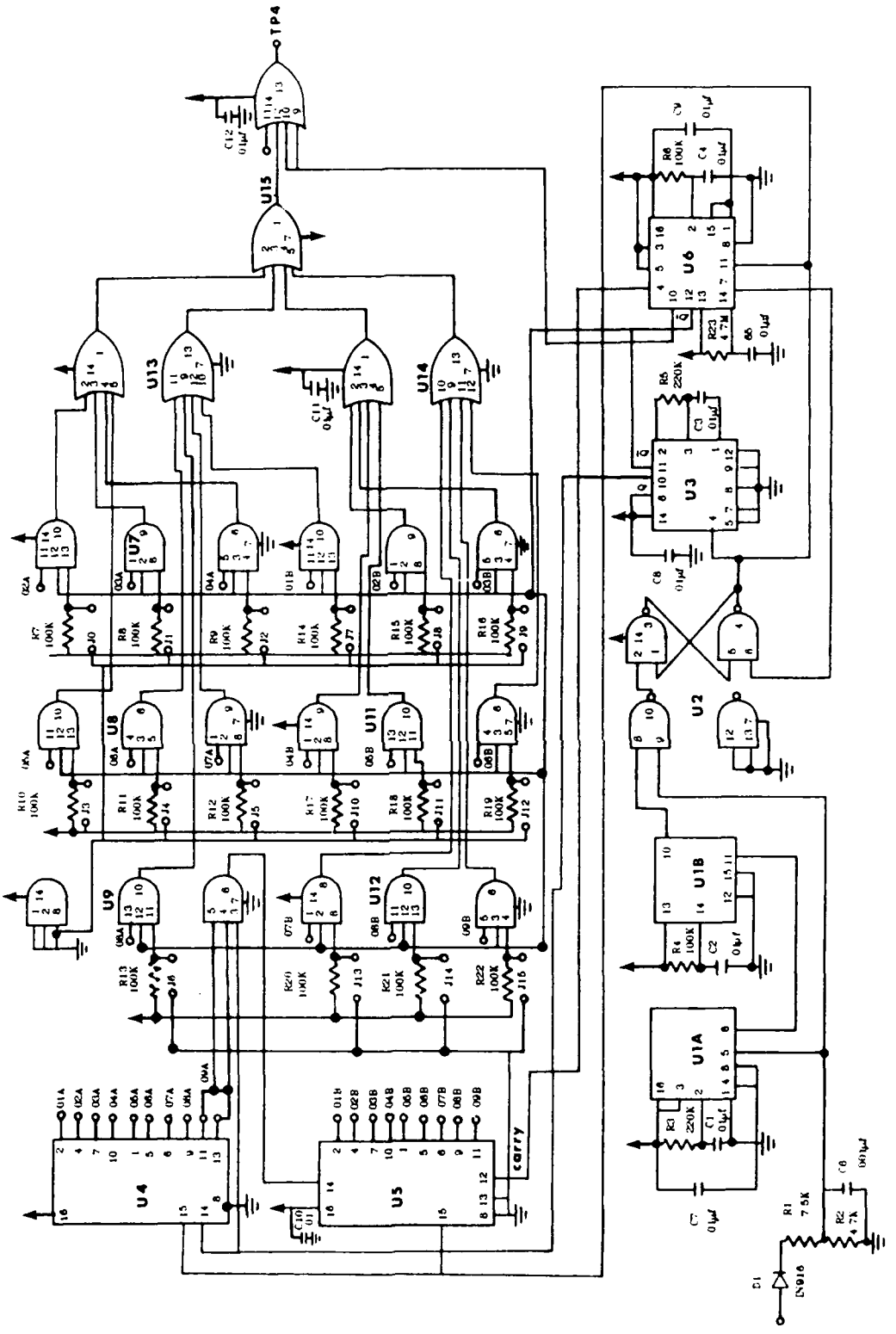


FIGURE 7 SERIAL IDENTIFIER SCHEMATIC

nine sequential parallel outputs, O1B through O9B and performs a "carry." The positive going edge of the "carry" output triggers a one shot (IC6A) producing a negative pulse to toggle the RS latch to its off state. EN goes high, turning off the MV and resetting both counters. Due to propagation delays and the use of "trigger" input on the MV, one additional cycle is output, which is ignored by the counters. It is later used to generate a stop recognition pulse.

Counter output O1A is used as a start recognition pulse. The remaining 16 outputs are used to generate a 16 bit serial code word multiplexed into the sensor amplifier. Each of the 16 code bits is AND'd with the Q output of the MV to produce a half width pulse and a hi or lo state to code a "1" or "0". (IC7 through IC12.)

The resultant code is in sequential parallel form. It is OR'd in IC13, IC14, and IC15 converting it to serial form. The start bit, O1A is OR'd in IC15 with the code. The stop bit is generated by EN going high, enabling IC6B which then triggers on the next (run-over) Q output. The one shot is set for a pulse of 150 ms, approximately 3 times the code pulse duration. This output is also OR'd in IC15. The output is a spaced serial or return to zero format. With the condition of low environmental activity this signal can be read by the computer. As an analog output it can easily be read in all except a very environmentally noisy signal.

The output of IC15-13 is: 1 start bit, 2 TC's duration;
16 code bits, each 1 TC duration;
1 stop bit, 3 TC's duration.

Power requirements 5 volts @ 2.1 ma (worst case)

Total time of the information scan is approximately 1.5 seconds. This signal (code) is applied to the positive input of the bridge amplifier through a 2 meg Ω resistor.

4.0 JUNCTION BOX SUBSYSTEM

4.1 CHAPTER OVERVIEW

This chapter covers the GDAS junction box and contains a functional, physical, electrical description complete with schematics.

4.2 PURPOSE OF EQUIPMENT

The junction box, its preamp/drivers, and calibration circuit are an outgrowth of need. Signal enhancement was the primary concern. The capacitance of the cables degraded the seismic signal by increasing the effective mass, thus changing its natural period. Transmission of the high impedance seismic signal over a long line, and injecting it into a high impedance amplifier left the system open to a multitude of noise sources. A similar problem existed in the calibration circuit. An extreme low level current (units of micro-amps) was impressed on the lines and reached the sensors as a poorly defined pulse, giving less than satisfactory results. These problems, among others, dictated the need for a total front end analog subsystem. This was the first major modification of the GDAS.

4.3 JUNCTION BOX FUNCTIONAL DESCRIPTION

As the name implies, the junction box is a central collection point for the various sensors. Within the J-box is complete circuitry to amplify, filter and condition the transducer signals for transmission to the recording site. The on board power supply has sufficient reserve to power remote and/or active sensors. A calibration system, intended for electro-mechanical calibration of the individual transducers, or electrical calibration of the entire amplifier system is also resident. A phone plug for a sound powered phone or similar system, is included. This in turn is wired (via cable) to an identical plug in the recording set to allow communications between the two sub-systems.

There are presently three models of the Junction Box. The older is a sixteen channel unit using a single nineteen pair cable for signal connection to the recording set. The other two are a modification of the older, designed to increase flexibility. One is a seven channel unit with one nine pair cable. The other being a sixteen channel set utilizing two nine pair cables. In the older system sixteen cable pairs are used for signal, one for calibration, one for communication and one spare. In the newer sets cabling was laid out for the increased flexibility. The first nine pair cable is divided into seven signal pairs, one calibration and one communication. This setup is identical for the seven or sixteen channel units. The other nine pair cable used with the newer sixteen channel unit contains nine signal pairs. With the signal conditioning line driving amplifiers there is virtually no limit to the distance between Junction Box and recording set. However a practical limit of 2000 feet is suggested. Table 5 presents full specifications of the J-box

Table 5 J-BOX SPECIFICATIONS

Internal Power Supply	Lambda MD-W-152
Voltage required	105-127 VAC @ .5 Amp 57-63 hz
Ambient Operating temperature range	0° to +71°C *
Storage temperature range	-55°C to +85°C
Output voltage (dual tracking)	
Adjustable range	±12 to ±15 volts
Regulation (line, load)	0.1%, 0.1%
Ripple mv RMS	1.5
Output Current (Amps)	±12v ±15v
40°C	3.1 3.3
50°C	2.8 3.1
60°C	2.3 2.6
70°C	1.6 2.0
Channel Capability	up to 7 or up to 16 plus calibration circuit
Input Connectors	
Power	Bendix PT07A 12-3 P
Transducer input	Bendix PT07A 12-10 S
Output connectors (either)	Bendix PT07SE 24-61 S
(or)	Bendix PT-7SE 18-32 S
Mating Connectors	
Power	Bendix PT06 SE 12-3 S
Sensor	Bendix PT06 SE 12-10 P
Output (either)	Bendix PT06 SE 24-61 P
(or)	Bendix PT06 SE 18-32 P
Temperature (Limited by power supply)	
Operating	0°C to 71°C
Storage	-55°C to +85°C
Mechanical Size	
Less connectors and mounting flanges	20" x 16" x 10"
Overall	24" x 17.5" x 10"
Weight	58 lbs.
Material	
Enclosure:	14 gauge type 304 stainless steel continuously welded.
Door Gasket:	Oil resistant neoprene with oil resistant cement.
Connectors (shell only):	Olive drab chromatic over cadmium over aluminum

* with output derating

4.4 JUNCTION BOX PHYSICAL DESCRIPTION

The J-box is built within a Hoffman 4X stainless steel electrical enclosure with a hinged door (Hoffman model # A 20H1610 SSLP) measuring 20"x16"x10". The door can be fastened for a full watertight environment and locked for security. Installation of sensor connectors has reduced the enclosure environmental integrity. These connectors are mounted as high as possible on both larger sides of the enclosure to avoid groundwater seepage and to preclude interfering with the door operation. Complete burial can occur but care must be taken to avoid percolation through the sensor connectors.

Within the J-box a card-cage rack and a Lambda LND-W-152 power supply have been built on a removeable panel. The power supply has the capability of powering the sixteen amplifiers as well as sufficient current to calibrate the seismometers or power remote preamps. Heat dissipation from within the J-box, both conductive and radiant, is adequate in all but strong direct sun. In hot climates, complete burial or ventilated shade (tenting) may be required.

The dual card cage has been built from two modified Scanbe "Rapid Rack" systems. They have been cut down to produce two nine position racks and are placed side by side within machined panels for a total of 18 places. Two edge connector trays, also modified, are wired for 16 channels of preamps and one calibration board. The other slot is intended for an extender card. Common lines (power, ground, calibration, and calibration return) are jumpered with bus bars. All other wiring is by point to point wiring, see schematics Figure 8 and Figure 9. The rack is mounted on a panel machined to be bolted into the box. Also mounted on the panel is the Lambda power supply. Wiring to and from the connectors will accommodate any of several standard wired transducers, either passive or active. Active transducers require a preamp card properly strapped to provide power to it.

The output of the individual amplifiers is wired to either a single 61 pin connector or two 32 pin connectors (original GDAS vs. hybrid GDAS.)

4.5 PREAMP/LINE DRIVER

4.5.1 PREAMP PHYSICAL DESCRIPTION

The front end amplifier (preamp) became a necessity in the GDAS. It has evolved from a simplistic single stage remote preamp to its present configuration of a multistage preamplifier, filter, line driver. A calibration circuit is also included having only the power in common with the amplifier. The entire subsystem was designed as an integral part of the J-box and is built on a 4.5 x 6.0 printed circuit board. A pair of test points has been mounted on the rear of the card for monitoring or set-up purposes. Two potentiometers allow for the adjustment of common mode rejection and DC balance. The board follows the schematic layout for ease in field adaption or repairs.

4.5.2 PREAMP CIRCUIT DESCRIPTION

The preamp/driver was primarily designed as a high input impedance seismic amplifier with integral transducer damping and low output impedance for driving long lines without signal degradation. It consist of three stages (see Fig. 10), the first of which uses A1 + A2 as a high impedance full differential amplifier. The second stage is a two pole lo-pass Butterworth filter, A3. The third stage, A4, is a buffer-driver used to decouple the circuit from the line. Also designed into this subsystem is a calibration circuit, A5, taking one of two configurations. Either a current source for seismometer calibration or a voltage

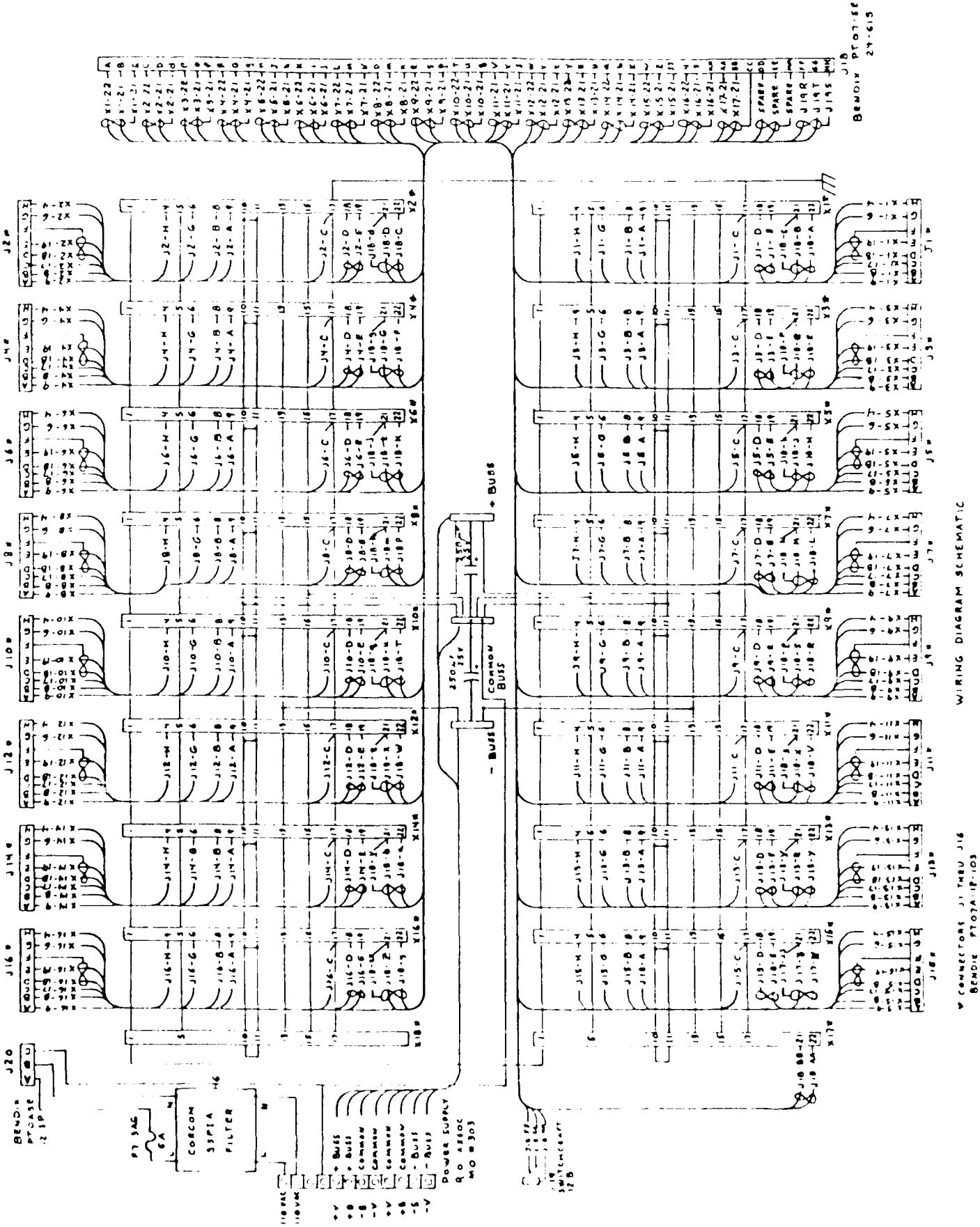


FIGURE 8 J-BOX WIRING DIAGRAM (OLDER)

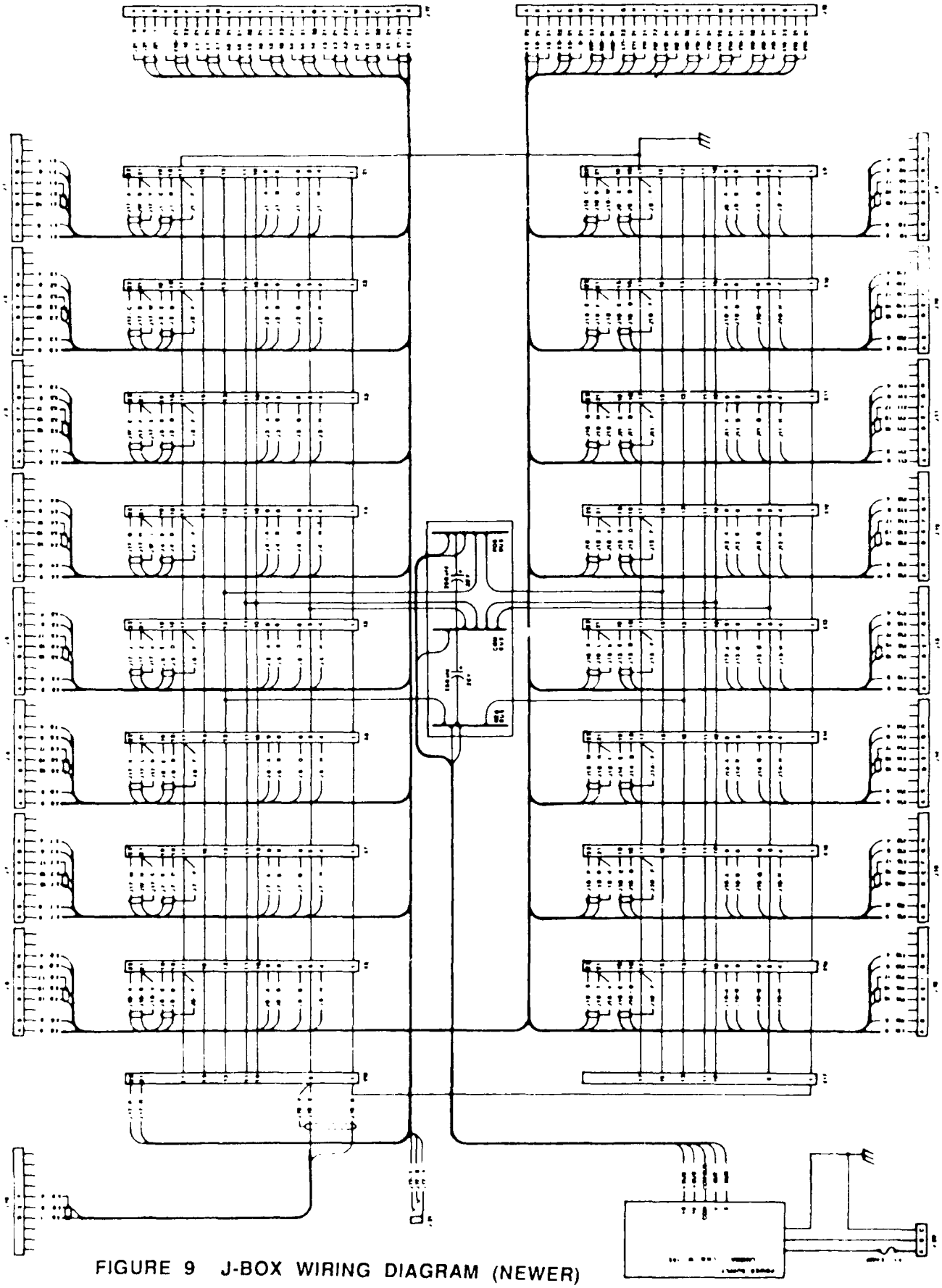


FIGURE 9 J-BOX WIRING DIAGRAM (NEWER)

comparator for interrogation or calibration of a bridge style transducer. The entire subsystem is built on a standard 4.5" x 6.5" printed circuit card with output test points. Complete specifications are given in Table 6.

The input stage is a high input impedance ($10^{10}\Omega$) differential amplifier with gain stepping resistors. It exhibits high common mode rejection which is not affected by gain changes. A potentiometer balances the gain of the two halves of the amplifier effectively nulling the common mode rejection. The circuit is inherently low drift particularly at the lower gains for which it is strapped. Further, resistor selection best balances the op amp differential input bias currents. Equal gains of A1 and A2 insure a cancellation of bias drift. Further, the single cross-coupled balancing resistor also reduces drift. (The additional circuits built on A3 and A4 are respectively non-inverting and inverting unity gain amplifiers and will cancel each others drift, assuming homogeneous temperature fluctuations.)

The resistor network (R1 thru R4) is fundamentally the damping resistor. The reasons for four resistors, all meant to be soldered in place for reduced noise, are many: First, the total damping resistor is the sum of the four. As represented, the damping is halved and balanced effectively forcing the seismometer or other transducer to be presented as a balanced source (i.e. a phantom ground is reflected in the source by virtue of the grounding of the junction of R2 and R4). The grounding of R2 and R4 presents the required D.C. ground return for the non-inverting input of A1 and A2, references the sensor to ground, and allows the use of a floated sensor. Also, in areas of high signal input, the damping can function as voltage divide network. The signal presented to the amplifier will be a fractional portion of the seismic signal.

$$\text{voltage divide} = \frac{R2}{R1 + R2}$$

$$\text{assuming} \qquad \frac{R1}{R2} = \frac{R3}{R4}$$

If desirable, this network can be configured as an RC combination, allowing high pass or low pass amplification. The combination would be a single pole filter determined by the equation:

$$\omega = \frac{1}{R1C1}$$

As mentioned, the selection of resistors with the A1, A2 circuit was to affect bias current balance and equal gain. In the final circuit, R5 is the common mode adjust. A rejection ratio of 66db was easily obtained. For differential balance:

$$\frac{R5 + R6}{R7} = \frac{R9}{R8}$$

The capacitors C1 and C2 were installed as oscillatory suppressors. They produce a cutoff frequency of approximately 6 Khz and therefore do not affect the common mode balance in the band of interest.

In operation, A1 is connected as a noninverting amplifier with a gain of 2.0 and is fed to A2 which has an inverting gain of 1.0 for a total circuit gain of 2.0. This equals the noninverting gain of A2 where the two inputs of the differential signal are combined for a single ended or ground referenced output.

$$\text{Assuming} \qquad \frac{R5 + R6}{R7} = \frac{R9}{R8} \quad \text{and further, } (R5 + R6) = R7 = R8 = R9$$

Differential gain = -AD = 1 + (R9/R8) = 2

$$\text{Common mode gain} = ACM = 1 - \frac{R5 + R6}{R7} \times \frac{R9}{R8}$$

Where, Vos = Vos (A1) - Vos (A2),
The total gain equation, or transfer function is given as

$$Eo = -AD\left(1 + \frac{ACM}{AD}\right)(ED + Vos) + ACM\left(ECM + \frac{Vos1 + Vos2}{2}\right)$$

which at balance reduces to Eo = -AD ED

Or; Eout = - Differential Gain x Differential Input Voltage

Note that the input voltage of A1 must be less than Req/Req + R9 times the output voltage, or 5 volts, thus limiting the common mode voltage to this value. As such, the common mode handling capability is reduced in inverse proportion to the first stage gain. The need for low gain and a low expected common mode signal plus the lower drift expectancy of equal resistors made this compromise worthwhile. This circuit can be redesigned for a higher common mode handling.

The circuit gain can be changed by the addition of a single resistor jumpering the two summing junctions (negative inputs) of A1 and A2. This resistor will increase the differential gain, but not the common mode gain. Therefore, the common mode balance and handling capability will remain constant with gain changes. This resistor affects both halves of the amplifier equally, holding the drift cancellation mentioned earlier. For gain purposes, this resistor, RG, is effectively across (R5 plus R6), and R9.

In that R5 + R6 at balance = 20 k = Req. the gain of the circuit is given by

$$G = AD + \frac{Req + R9}{R\,G}$$

Where: G = total gain and Req = R9

AD = differential gain of the primary circuit

AD = 1 + R9/R8 = 2

$$G = 2 + \frac{40k}{R\,G} \quad \text{and} \quad RG = \frac{40k}{G - 2}$$

Provisions are made on the board for 5 gain changes. Resistors R10 through R14 and jumpers J1 through J5 produce 6 binary gain steps of 2, 4, 8, 16, 32, and 64.

The following stage is a unity gain two pole Butterworth filter using A3 as an active element. This circuit is a standard form having the following transfer function:

$$Av + = \frac{Vo}{Vi} = \frac{1}{S2(C4C3R1R2) + S[C3(R1 + R2)] + 1}$$

For a two pole Butterworth, with 0.7 critical damping characteristics, R1 = R2, and C4 = 2C3, the filter equation is:

$$\text{Flopass} = \frac{1}{8.88\ R1\ C3}$$

On board provisions allow for 4 filter settings. One must be selected to pass the signal and the jumpers J 6A,B through J9A,B, must be made in pairs. These filter settings are 100hz, 200hz, 500hz and 1000hz, respectively.

The output stage is an inverting unity gain amplifier. Resistor R26 equals the parallel combination of R24 and R25 for least bias drift. Capacitor C5 suppresses oscillations. R27 decouples the op-amp from the large capacitive load presented by the long signal lines and hence the circuit is used as a line driver. This resistor is within the feedback loop of the op-amp and is effectively reduced by the feedback gain which sees it as part of the output impedance and prevents its appearance as a finite resistor in the line. This circuit can, as was intended, to be used for additional amplification if desired.

Where; $\text{Gain} = \frac{R25}{R24}$

Care must be exercised to prevent load of filter A3. It is suggested that

$R24 > 10\ k$ and

$R26 = R24 \parallel R25$ for best bias and drift.

Table 6 PREAMP/LINE DRIVER SPECIFICATIONS

Amplifier type	non-inverting.
Input Impedance*	
Differential	$10^8\ \Omega$
Common mode	$10^{10}\ \Omega$
Gain by Jumper selection	
No Jumper	2
Jumper J1	4
Jumper J2	8
Jumper J3	16
Jumper J4	32
Jumper J5	64
Gain accuracy	
Absolute values	4.0%
Computed values	1.5%
Low Pass Cutoff Frequency	
Jumper J6A,J6B	100hz
Jumper J7A,J7B	200hz
Jumper J8A,J8B	500hz
Jumper J9A,J9B	1000hz
Filter accuracy	5%
Total Noise RTI	< 2 μv pp 0.1-10hz
Total Drift RTI	< 5 μv/°c
Output Impedance	< 0.1 Ω
Common Mode Rejection (CMRR)	> 66db DC-50hz

* Not including damping resistors

4.5.3 CALIBRATOR

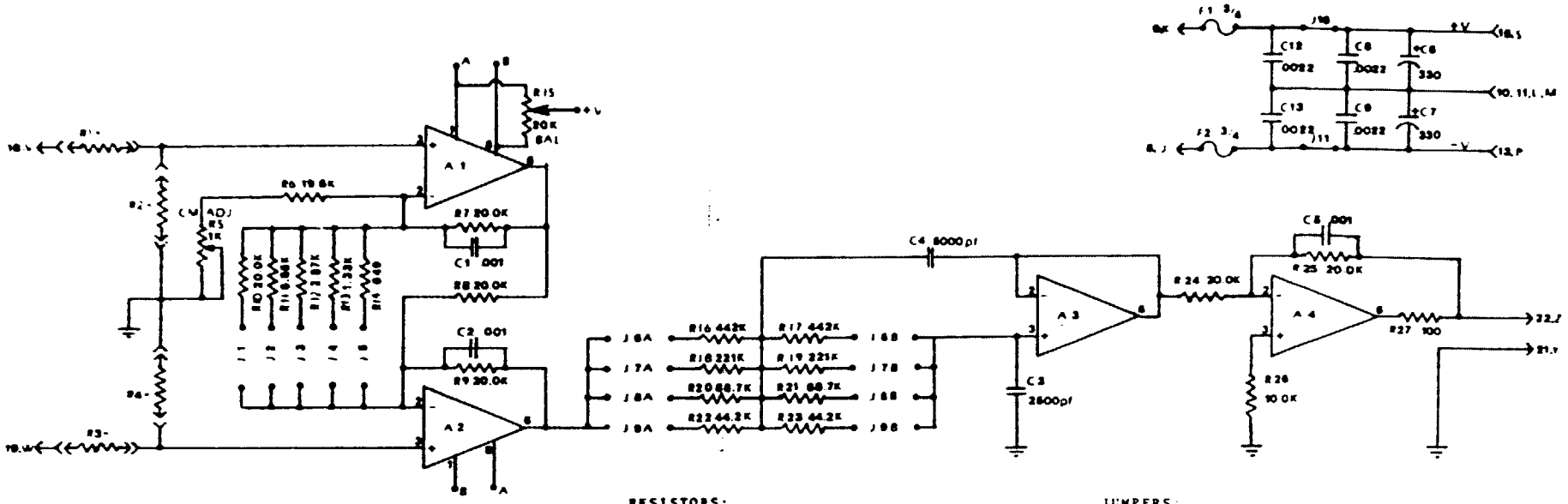
Built on one corner of the Line Driver Card and shielded from the rest of the circuitry is a single stage calibrator. Originally designed as an accurate current converter, a newer modification allows this circuit to be used, jumper selectable, as either a current converter or a voltage comparator, see Figure 10 and Table 7. When used as a current converter, the load is placed within the feedback loop. The op amp is forced to maintain a nodal voltage at the junction of R29 and R30 in a direct gain ratio to the input voltage. This requires the circuit to supply a constant current in direct relation to the input voltage through the load regardless of its impedance. A complimentary-symmetry amplifier located within the feedback loop is used to supply the required current. Its gain fraction is totally corrected for by the action of the loop, raising both the current capability and the effective driving impedance of the current converter. R31 and R32 are used to prevent thermal runaway of the complimentary pair. C10 prevents oscillations. C11 in conjunction with R29 produces a high cutoff frequency of 2500hz.

When used as a voltage comparator the purpose of this circuit is to supply a voltage with current capable to activate a relay in the transducer. The comparator can assume only one of two states. The biasing of the noninverting input by the voltage divider R30, R33, holds it in a high positive state (approx. +12v) and determines the transition level. When a voltage more positive than this bias is applied to the inverting input, the amplifier, by its high gain, switches near instantaneously to a negative level (approx. -12v) and will remain there until the input falls below the bias level. The complimentary-symmetry pair supplies the higher current required by the relay. The comparator has purposely been designed without hysteresis.

Required changes for these options are reflected in the schematic.

Table 7 CALIBRATOR SPECIFICATION

As a Current Source	
Op Amp	µa714HC/OP-07C
Input Impedance	R28
Output Impedance	> 10 MΩ
Conversion Equation	$I\ out = \frac{Ein}{R28}\left(1 + \frac{R29}{R30}\right)$
Current Limitations	
Max Load Impedance	1500
Output Current	
Design	35 ma
Absolute	65 ma.
Restriction	I out x R30 < 10 volts
Offset Current	< 0.5 µ
As a Voltage comparator	
Op Amp	µa 101 HM
Trip voltage range	+100 mv to +10V
Etrip	$15V\ \left(\frac{R30}{R33 + R30}\right)$
Current capability	65 ma
Slew time	100 µ sec.
Hysteresis	none (~60mv)



RESISTORS:

R27,R30 and R33 in Bridge Calibrater
RC07kw,5%

All Others: RN55C

CAPACITORS:

C3,C4 DM19 Mylar,5%
C6,C7 Tantalum

All Others: 7XR Ceramic

OP-AMPS:

A1,A2,A3 and A4	ua714HC/OP07C
A5 Seismic	ua714HC/OP07C
A5 Bridge	ua101HM

JUMPERS:

J1-J5 determine gain of 1st stage:

JUMPER	GAIN	GAIN EQUATION
None	2.0	AV=2+(40k/Rg)
1	[illegible]	where Rg=R10-R14
[illegible]	8.2	
[illegible]	[illegible]	Do not use more than one
[illegible]	[illegible]	jumper without recompu-
[illegible]	[illegible]	ting gain
5	64.0	

J6A,B-J9A,B:Determine upper cutoff frequency of 2 pole Buttervorth filter,A3:

JUMPERS	FREQUENCY	FILTER EQUATION
J6A,B	100 Hz	$F_{hi}=1/8.88RC3$
J7A,B	200 Hz	
J8A,B	500 Hz	
J9A,B	1000 Hz	

MUST BE USED IN A,B PAIRS

* Resistor values selected for field application:

R1,R2,R3,R4: Used to set damping value for seismometer where: R4=R1+R2+R3+R4
Used to set fraction gain via voltage division= R2 where: R1 R3
R1+R2 R2 R4

R28,R30 (Seismic): Used to set seismometer calibration current in conjunction with R29
Ical = (Ecal/R28) (1+30.1k/R30); constraint:IcalxR30 ≤ 12v

R30 (Bridge): Used with R33 to set trip point of comarator A5 Etrip= $\frac{R30}{15k+R30}$(15v)
minimum value 50Ω, =.05 volts

FIGURE 10 PREAMPLIFIER SCHEMATIC

4.6 CALIBRATION RECEIVER

4.6.1 CALIBRATION RECEIVER PHYSICAL DESCRIPTION

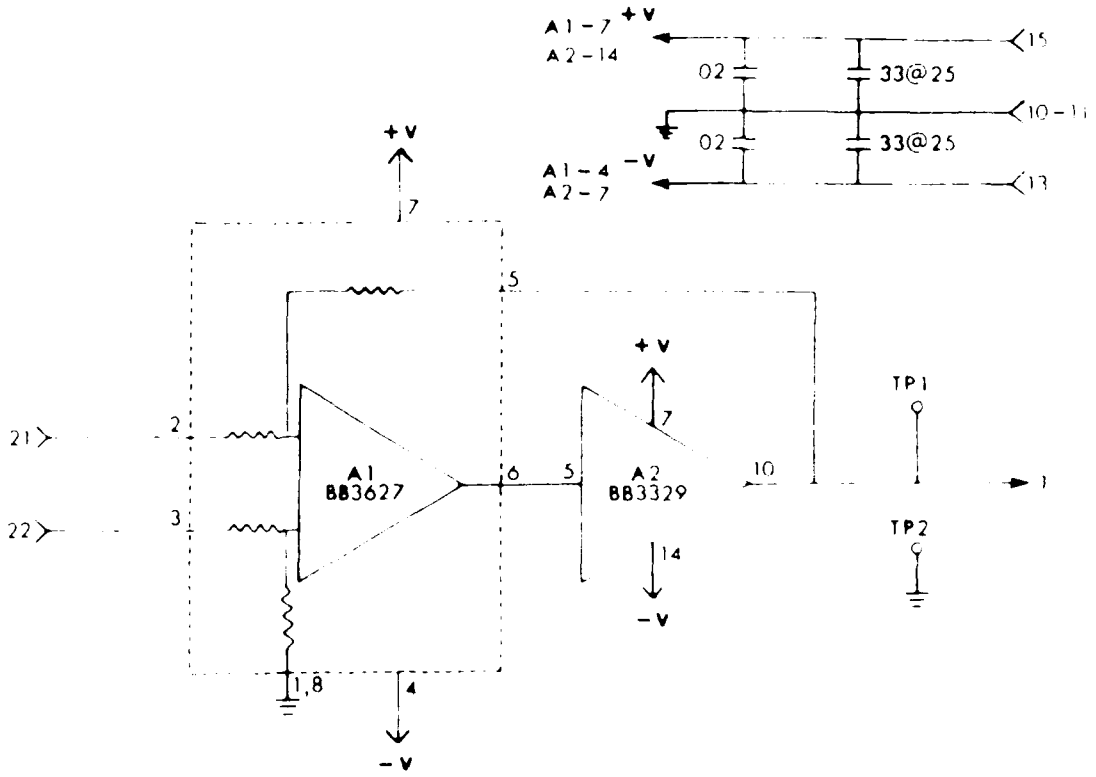
The calibration receiver board consists of 4.5 x 6.5 printed circuit card and operates in a special slot within the J-box.

4.6.2 CALIBRATION RECEIVER CIRCUIT DESCRIPTION

The calibration receiver card is comprised of a unity gain differential amplifier with a power booster, see Figure 11 and Table 8. Its function is to disconnect the calibration source (i.e. the computer driven D.A.C.) from the circuitry within the J-box, and also to present a minimal load to that source. The differential amplifier, Burr Brown #3626AM is totally contained (resistors and op-amp) within a TO-5 can and is laser trimmed for offset and gain accuracy. The power booster, Burr Brown #3329/03 is capable of supplying up to 10 volts @ 100 ma. This booster is installed within the feedback loop of the op amp negating any inaccuracies it may have. Output from this card is bussed via the J-box wiring to the other seventeen card slots for use in the calibration circuits of the preamp/driver board and subsequently by the sensors, as a calibration current or voltage. It is also wired to an external connector for a full system calibration.

Table 8 CALIBRATION RECEIVER SPECIFICATIONS

Input Impedance	50 k
Input voltage range for linear operation	
Differential	±10V
Common Mode	±20V
Common mode rejection, DC-60hz	90db
Gain equation	1V/V
Gain Error (all cases)	<±0.01%
Rated output	±10V @ 100 ma
Offset R.T.O. (max.)	<250 μ volts
Noise Voltage R.T.O. (0.01hz-100hz)	<3.5 μ volts
Full power Bandwidth	14 Khz
Small signal 1% flatness	5 Khz
Operating and Storage Temperature	Limited by J Box



CALIBRATION RECEIVER/DRIVER

FIGURE 11 CALIBRATION RECEIVER SCHEMATIC

4.7 INTER GROUP CABLING

Cabling used between the J-box and recording site is multi twisted pair cable. Each pair is fully shielded. Each shield is insulated from adjacent shields and has a drain wire associated with it. In this fashion, each pair is not only shielded from outside interference, but from crosstalk interference with neighboring pairs. Also, with a properly made cable, no multiple ground paths (shields) exist.

Figure 12 shows the pin layout and wiring order of the connectors associated with the cabling. The connector is further outlined to make pair location easier.

These cables have purposely been made male to male to allow for easier field use. A female to female jumper cable must be used to interconnect multiple lengths. The predominant cable used is Belden #8700 series. However, any cable meeting or exceeding the specifications will suffice.

BENDIX PT**-*-18-32*

PIN	PAIR NO.	WIRE COLOR
A	1	Red
B	1	Black
V	1	Shield
C	2	White
D	2	Black
W	2	Shield
E	3	Green
F	3	Black
X	3	Shield
G	4	Blue
H	4	Black
Y	4	Shield
J	5	Yellow
Z	5	Black
a	5	Shield
K	6	Brown
L	6	Black
b	6	Shield
M	7	Orange
N	7	Black
c	7	Shield
P	8	White
R	8	Red
d	8	Shield
S	9	Green
T	9	Red
e	9	Shield

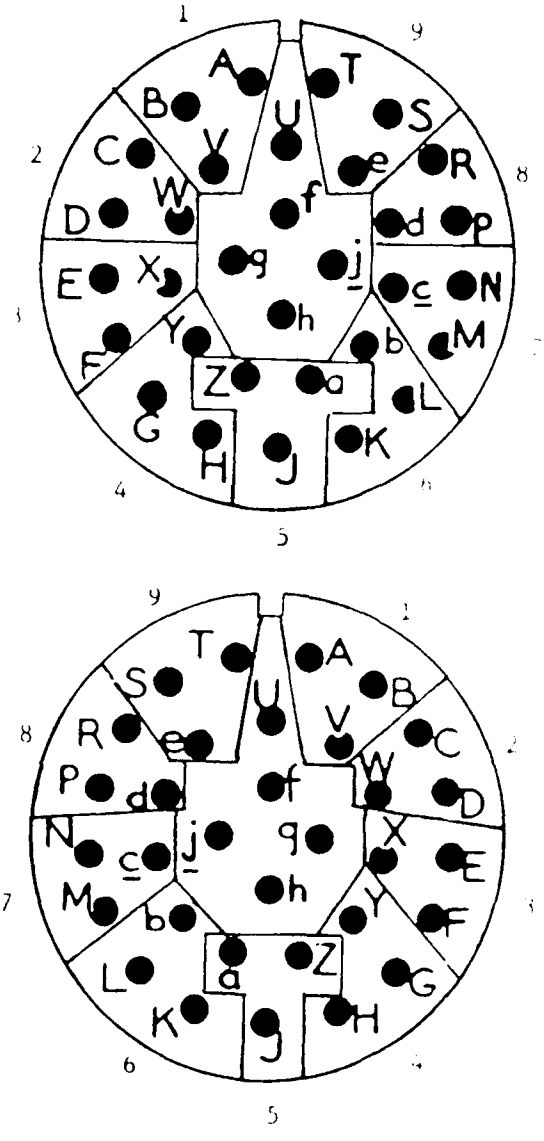


FIGURE 12 INTERGROUP CABLING PIN DESIGNATION

5.0 SIGNAL CONDITIONING SUBSYSTEM

5.1 CHAPTER OVERVIEW

This chapter covers the signal conditioning subsystem. It begins with a function description and follows with a description of the physical components of the unit, including modifications, theory of operation and circuit diagrams. The final part of the section deals with the software that has been developed to configure the subsystem and to determine its actual operational characteristics.

5.2 SIGNAL CONDITIONING FUNCTIONAL DESCRIPTION

The signal conditioning subsystem receives the analog information from the remote J-boxes and routes the selected channels to an amplifier/filter system for subsequent digitation and recording.

The subsystem consists of a switch box which is a means of receiving multiple J-boxes and selecting those outputs to be recorded. The amplifier/filter section consists of a rack of 16 single channel analog signal conditioners, each of which is on a separate printed circuit board. These boards can individually be set up for various filter types.

The rack also contains a calibration driver circuit mounted on a printed circuit board to assist in the calibration, set-up, and troubleshooting of the system.

5.3 SWITCH BOX

The switch box is a new subsystem designed for the VAMS with the intention of incorporating it into the GDAS. It allows for the flexibility of multiple J-boxes, widened and varying an array or arrays and serves as the terminus for the J-box cabling (see Figure 13).

A maximum of three J-boxes can be used simultaneously with the GDAS, 1 sixteen channel and 2 seven channel, or 3 seven channel. There are 4 multipin connectors on the bottom of the unit. J1 and J2 connect the two cables from a 16 channel box, or J1, J3, and J4 are wired to service three 7 channel units, J2 is then unused. These connectors, with a total of 30 possible channels, are wired to a series of terminal strips inside a drop-front panel on the front of the unit. Selection of the 16 channels to be processed is made by attaching coded wiring to the terminal strips with installed quick disconnect push plugs. These wires then route the signals to a four slot card cage built into the box. This card cage was designed into the system to allow for future expansion. It is totally wire, but lacks a power supply and circuitry for operation. Printed circuit boards have been designed and laid out, but not fabricated, and will allow for decoupling and amplification of the signals in an envisioned future update. At present, two jumper cards must be installed for signal continuity. The output of the card cage is wired to a 37 pin "Delta" connector on the back panel. This mates with an 18 twisted pair ribbon cable and delivers the signals to the conditioning amplifiers.

The calibration signal, originating in the conditioning amplifier subsystem, is hard wired through the switch box to the J-box connectors allowing simultaneous calibration of all J-boxes.

The phone jack for the recording site voice communications is mounted on the rear panel and is also wired to the J-box connectors for use to all of the J-boxes.

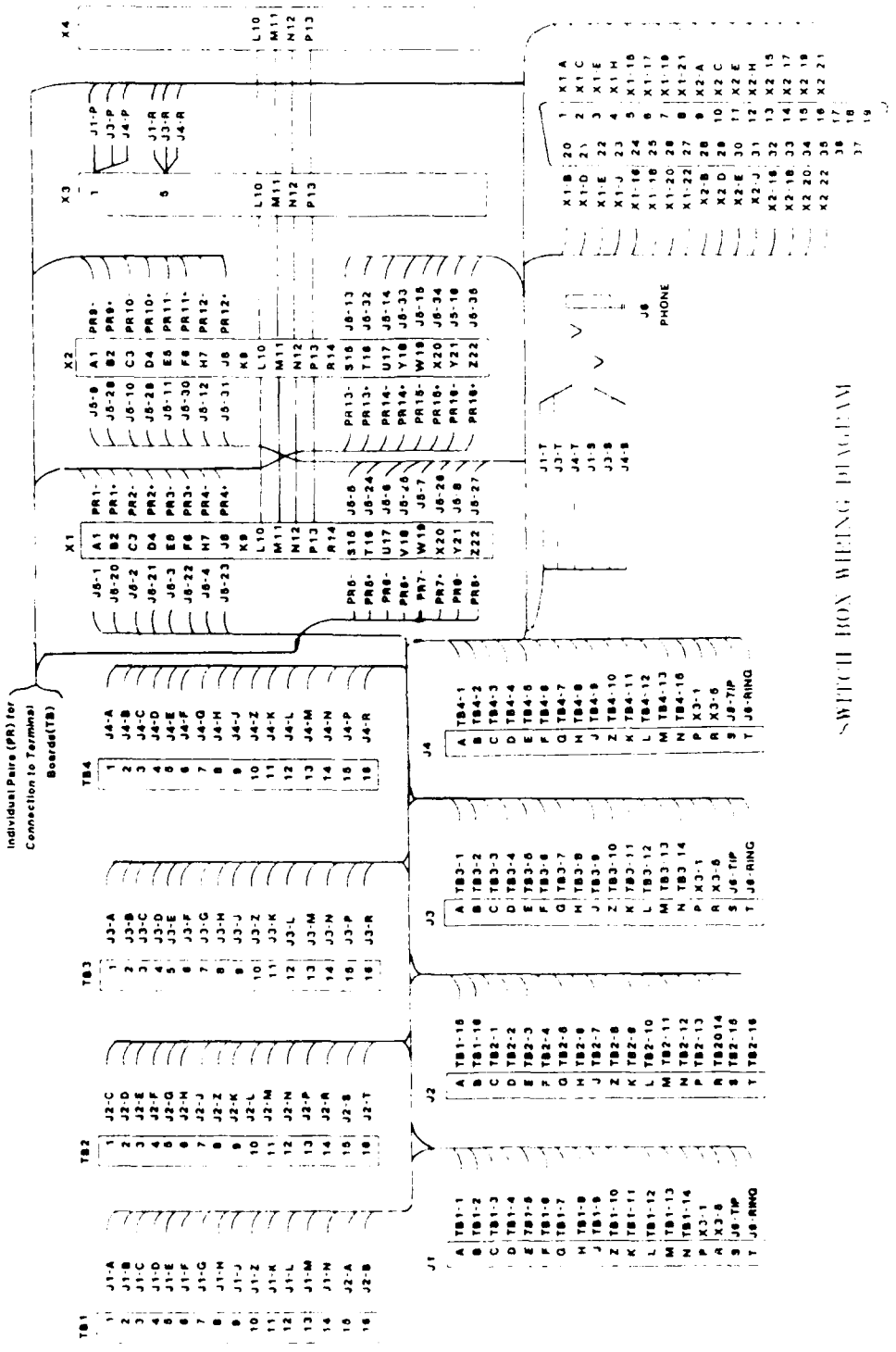


FIGURE 13 SWITCH BOX WIRING DIAGRAM

The switch box is built into a modified Scanbe "Card Cage" and requires 5.25" of panel space. It is intended to be back mounted in the equipment rack with accessibility to its back panel. Cable connection to the bottom of the box requires a minimum of 6" of space below the unit.

5.4 AMPLIFIER/FILTER SUBSYSTEM

5.4.1 AMPLIFIER/FILTER CHASSIS

The amplifier/filter chassis (filter deck) is the terminus of the entire analog section: sensors; preamps; J-box; amplifiers. Its purpose is to house the signal conditioning cards that relay the J-box signal to the analog to digital converter (ADC). The rack system housing the amplifier boards is an open face unit allowing free access to the amplifier boards. The power panel contains a power-switch, pilot lamp, and supply voltage test points. This unit requires 5.25" of height in a standard 19" rack. The seventeenth position in the rack system houses a calibration driver board. Its purpose is to decouple the calibration source and condition the signal for long line transmission to the J-box.

The older (SDAS) deck has been completely rebuilt, encompassing a new linear power supply and total rewiring in a successful noise reduction move. In reducing the wiring bulk and complexity, the unused options in the deck were deleted. This included the recorder output and the unused signal combination slot. Early in the modification scheme the seventeenth slot was dedicated to a multi-use calibration circuit, and a card was built for that purpose. The deck now consists of 16 amplifier channels and one calibration circuit.

Mechanically the Vector card rack was rebuilt, both strengthening it and improving the shielding aspect afforded by the metal structure. From a physical point of view the order of the amplifiers was reversed to the more accepted left to right counting with the power panel on the left side and the calibrator in the 17th or final slot. The power supply is mounted inboard of the new rear panel, reducing the depth to 15.75". The uncluttered rear panel now contains an input and output connector (37 place Delta), a power cord, and single fuse.

The back plane, or edge connector tray, is bus wired for power. This in turn receives remotely sensed voltage from the subsystem power supply complete with decoupling capacitors, electrolytic for low frequency and ceramic for high frequency noise. The input and output connectors are wired for full differential operation with twisted pairs. No cable shielding has been brought in to the unit, further reducing noise sources.

As previously mentioned, the card cage contains 17 positions, 16 for the filter-amplifier cards. The input of these cards is routed from the output of the J-box preamps/drivers. A full description follows in the next paragraph. The 17th position is used for a system calibrator. Depending on switch position and connections the circuit can calibrate all or portions of the GDAS, and can be used as a diagnostic or trouble shooting aid. This aspect will be discussed in the calibration circuit paragraph.

The signals from the individual amplifiers are wired to the output connector with separate signal returns to reduce cross talk that would occur on a common line. These signals are then routed to the analog to digital converter (ADC) via twisted pair to reduce the likelihood of induced noise. Figure 14 is a wiring diagram of the filter deck.

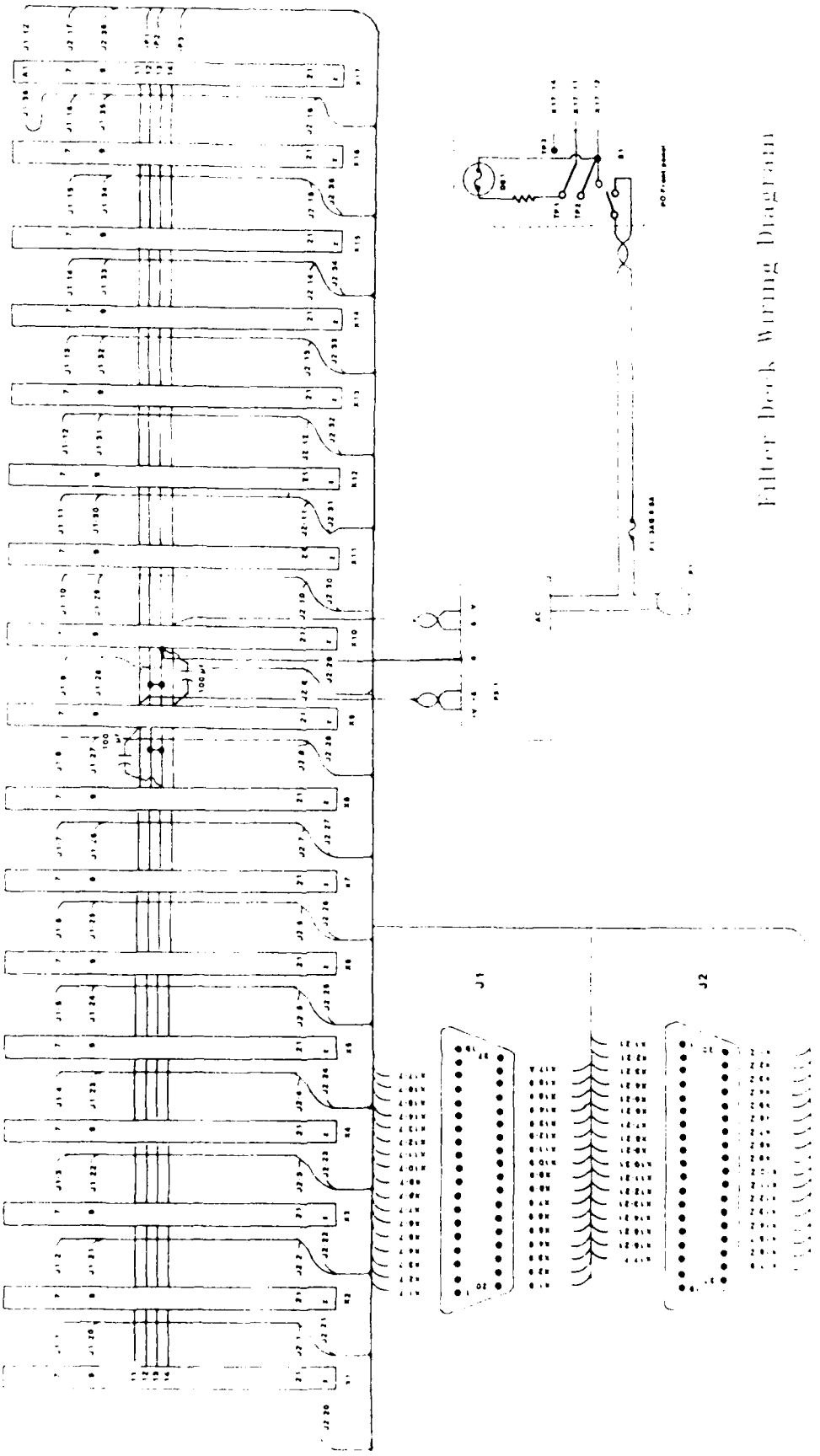


FIGURE 14 FILTER DECK WIRING DIAGRAM

5.4.2 AMPLIFIER/FILTER CIRCUIT BOARD DESCRIPTION

5.4.2.1 CIRCUIT BOARD PHYSICAL DESCRIPTION

Each amplifier/filter card consists of a 4.5 x 10 in. fiberglass printed circuit board. Permanently mounted on the board are the amplifiers and certain components used to form the filter and gain sections. The exact configuration of the filters is determined by header-mounted components that plug into the four vacant integrated circuit sockets visible on the card. Each board can be configured to provide various types of signal conditioning filters including lowpass, highpass, bandpass, and anti-aliasing. The board also has an overrange circuit to provide a visual indication of signal clipping. A set of test points has been included for monitoring the signal at various points in the filter chain. Mounted near the test point are a trimpot for adjusting circuit dc offset and a light emitting diode (LED) for indicating overrange signals.

5.4.2.2 AMPLIFIER/FILTER CIRCUIT BOARD MODIFICATIONS

The amplifier/filter board has undergone only minor modifications in its years of use. Among these is an input filter, used to reduce the interaction of the older switching power supplies used in the J-box and filter deck. With the rebuilding of the analog section and the replacement of these supplies the modification is no longer needed for the purpose intended. However, it has been noted in field use that the input instrumentation amplifiers are extremely sensitive to charge fields (near lightning strikes, static, etc.) and those units not exhibiting a total failure due to this abnormality are likely to be noisier and/or tend to oscillate with high input levels or a heavy capacitive load. This is most likely due to a stressing of the circuit to substrate junction due to the high energy level and will result in ultimate failure. The filter modification, mentioned above, tends to reduce this problem and field failures have greatly lessened since its inclusion in the circuit.

Another modification concerns the physical building of the filter components. Mounting of the component on single component carrier was extremely flexible but also noisy and subject to greater human error and component loss. The carriers were subject to vibration and hence to poor connections and resultant noise. Presently the filter components are mounted on a single header per filter. The result is a much tighter quality connection with less vibration induced noise, less chance of wrong component errors and no lost components.

The main modification is the use of the circuit. The filter card is now almost exclusively used as a single stage instrumentation amplifier followed by a 6 pole anti-aliasing filter. References in circuit analysis caution against using cascaded filters for gain. Note that this arrangement is not prohibited. Total system gain, preamp and frontend amplifier, can be as high as 100,000 volts/volt or 100db, making minor adjustments in the filter sections unnecessary.

5.4.2.3 AMPLIFIER/FILTER CIRCUIT DESCRIPTION

Figure 15 is a block diagram of the amplifier/filter board. Each card consists of five conditioning stages, output buffers, and an overrange indicator. Detailed circuit diagrams and circuit descriptions follow in another paragraph.

Stage 1 consists of a variable gain instrumentation amplifier. The amplifier features a differential input with high common mode signal rejection to minimize the effects of noise picked up in the cable from the junction box. It functions as an input buffer, isolating the following stages from interaction with the input signals. It also provides signal

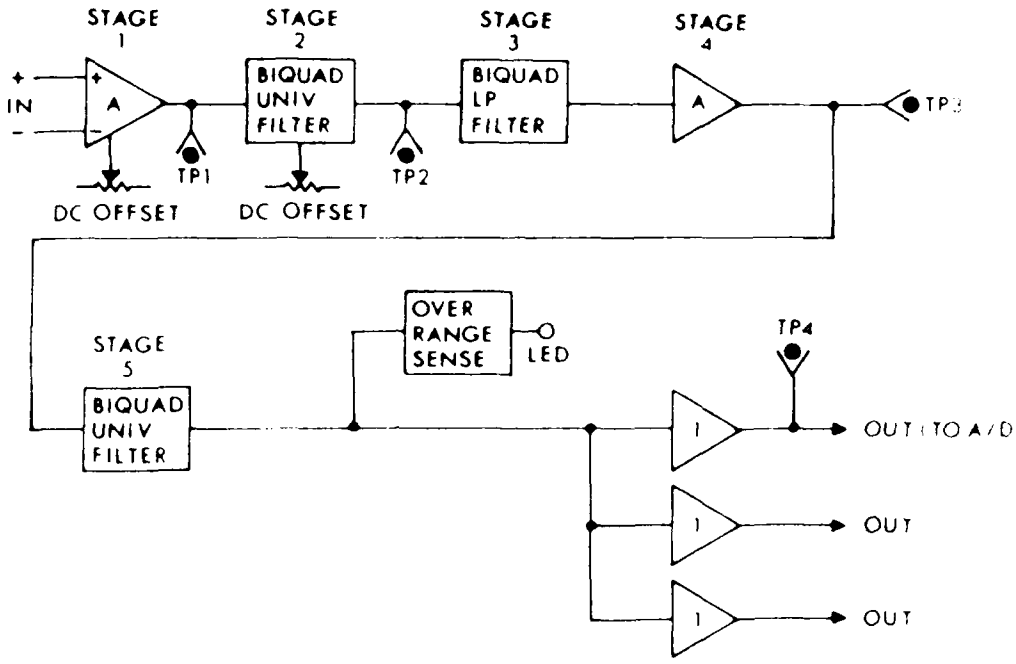


FIGURE 15 AMPLIFIER/FILTER BLOCK DIAGRAM

gain as set by two resistors, R101 and R102, located near the amplifier on the circuit card. A dc offset adjusting trimpot is located near the amplifier for nulling out any input offset voltages. The high frequency response of the amplifier is limited by a resistor/capacitor network. The network inserts a pole at approximately 677 Hz.

Stages 2, 3, and 5 are similar. Each consists of amplifiers and certain fixed components needed to form biquadratic (biquad) universal active filters. Each filter stage can provide a second order lowpass, bandpass, highpass, allpass, or band reject filter. (See precautions in preceding paragraph.) Stages 2 and 3 differ slightly from stage 5. Stage 2 has an additional dc offset voltage adjustment via a trimpot located on the outside edge of the card. This adjustment allows the user to correct for dc drift or offset of signals amplified by the card. Stage 3 is set up as a lowpass filter only. It can handle lower frequencies than the other two stages through the addition of extra capacitors (using solder pads included for that purpose). All parameters for these filters (filter type, gain, frequency response, damping coefficient) are set by header-mounted resistors plugged into the board. Section 5.5.2 of this report covers software developed to assist in the selection of these resistors.

Stage 4 is an amplification stage. Its gain is set by two resistors. Also, by the addition of a capacitor in parallel with one of the resistors, the stage can provide a single lowpass pole. (See precautions in preceding paragraph 5.4.2.2)

Three independent buffered outputs are provided on the board. They appear on the board's edge connector and are single ended. One supplies a signal to the A/D converter, the others are presently not used.

A visual overrange indication has been built into each board. The indicator uses a buffered comparator to monitor the boards output and turn on the LED when the output exceeds approximately +10 or -10 Vdc. This level corresponds to the maximum input signal level of the A/D converter. Thus the user is given a visual indication of possible A/D signal clipping.

Four test points have been incorporated into the board. These appear, together with system ground, on a multiple test point module on the edge of the board. They give the output stages 1, 2, 4, and 5, with the stage 5 output paralleling the signal recorded by the A/D. At these points, one can measure dc offset and observe the signal waveform using a voltmeter or an oscilloscope.

Caution: The stage 1 test point should be monitored using a 10x oscilloscope probe only. Lower impedance probes may cause the stage 1 amplifier to oscillate.

Table 9 summarizes the features of each conditioning stage; Table 10 gives specifications for the signal conditioning board.

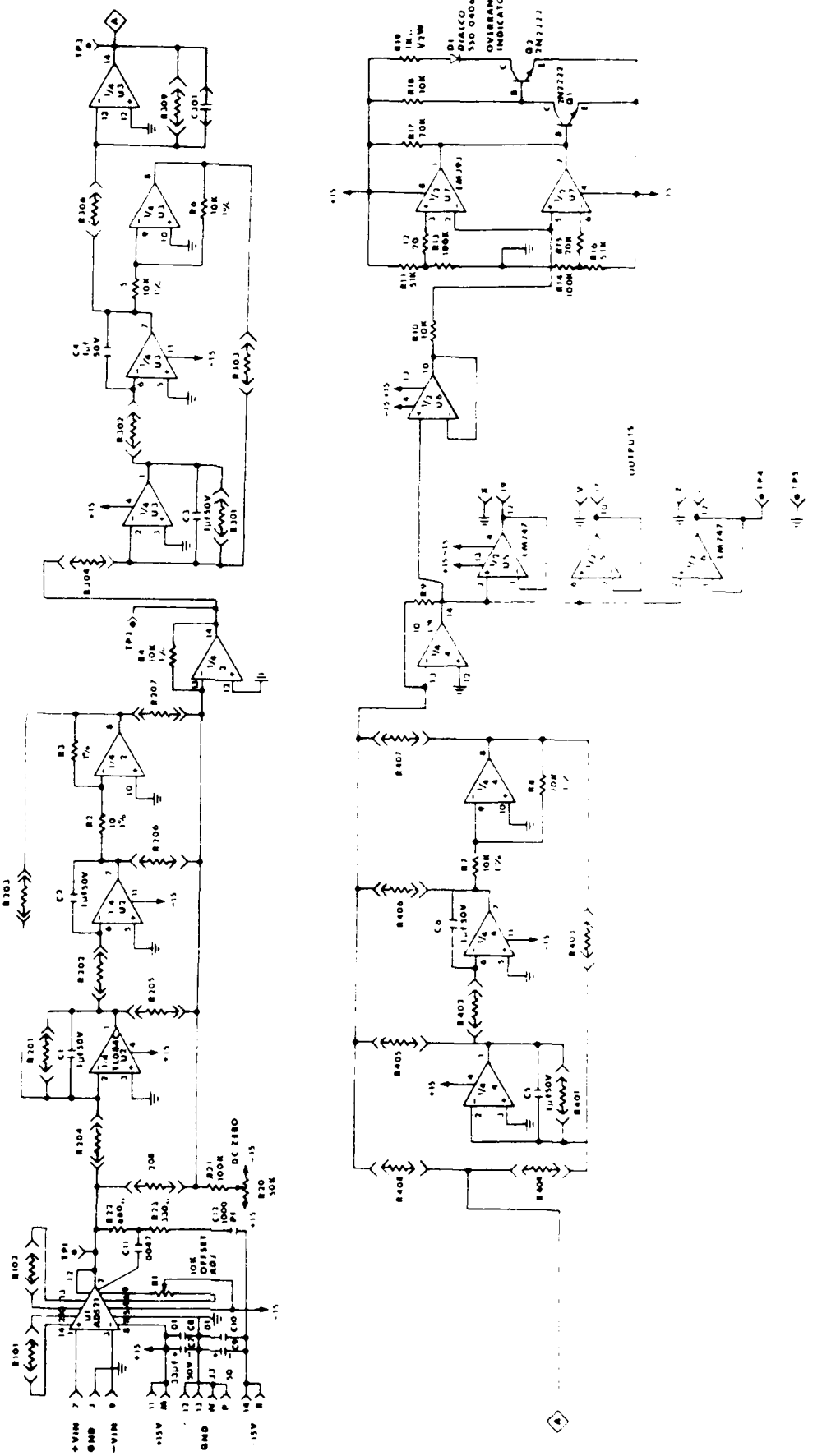


FIGURE 16 AMPLIFIER/FILTER SCHEMATIC

Table 9 AMPLIFIER/FILTER FEATURES

Stage	Features
1	Variable gain, differential input, instrumentation amplifier Dc - 677 Hz frequency response Input offset null adjustment Output fed to card edge test point
2	General purpose (LP, HP, BP, BR, AP) biquad filter Dc offset adjustment (via pot. at card edge) Output fed to card edge test point
3	Lowpass biquad filter Capability than stages 2 and 5 Additional filter capacitors easily added
4	Amplification only (not recommended) Can add capacitor for one lowpass pole Output fed to card edge test point
5	General purpose (LP, HP, BP, BR, AP) biquad filter
Output	Three individually buffered outputs (one fed to card edge test point) LED overrange indicator

Table 10 AMPLIFIER/FILTER SPECIFICATIONS

Input Impedance	3000 Megohm II 1.8 pF
Input CMRR	100 dB, min.
Input Noise	10.0 μv (P-P, dc - 200Hz)
Max Input Voltage For Rated Performance	± 10Vdc
Max Input Voltage Without Damage	± 30Vdc (each input to be ground)
Output Saturation Level	± 12 Vdc
Harmonic Distortion	0.5% @ 12 Hz input
Output Impedence	< 0.001 Ω

5.4.2.4 AMPLIFIER/FILTER CIRCUIT FUNCTIONAL DESCRIPTION

Figure 16 contains the schematic diagram of the signal conditioner circuit card.

Amplifier U1; together with R1, R22, R23, C11, and C12; makes up stage 1 of the conditioning card. Stage gain is set by the values of R101 and R102 which plug into socket XR1. Components C11, C12, R22, and R23 make up a compensation network to prevent high-frequency oscillation. R1 allows for nulling of the stage dc input offset.

Stage 2, a universal biquad filter, is made up of U2 and associated components. R2, R3, R4, R20, R21, C1, and C2 are soldered to the board. R20 and 21 allow dc offset adjustment for the entire card. The dc value set by the wiper on R20 is added to the filter output and amplified by the rest of the card. R201-R208 are mounted on a header and plugged into socket XR2.

Three of the four sections of U3 make up stage 3, a biquad lowpass filter. R5, R6, C3, and C4 are soldered to the circuit board. Extra solder pads have been provided in parallel with C3 and C4 to allow addition of capacitors to lower the frequency range of the stage. R301-R304 are mounted on a header and plugged into socket XR3.

The fourth section of operational amplifier U3 is used to form stage 4 of the signal conditioning card chain. Its characteristics are set by R306, R309, and C301, mounted on the header which plugs into socket XR3.

The four sections of U4 are used to make up stage 5, a universal biquad filter. R7-R9, C5, and C6 are soldered to the board. R401-R408 plug into socket XR4.

Unity-gain buffers for the board outputs are provided by U5 and U6. Half of U6 is used to buffer the input to the overrange sensing circuit.

Dual comparator U7 and associated components make up the overrange sensing circuit. U7 is set up as a window comparator with a range of approximately +10 to -10 Vdc set by R11-R16. When the input voltage is outside the window, Q1 and Q2 turn on the overrange indicator D1.

5.4.3 SYSTEM CALIBRATION DRIVER CIRCUIT

5.4.3.1 CALIBRATION DRIVER PHYSICAL DESCRIPTION

This circuit consists of a hand built, pre-punched 4.5 x 10 in. fiberglass board. An input selector switch allowing either computer or local input, and measurement test points are mounted on a front panel. Components are minimized due to the complexity of the analog integrated circuits used.

5.4.3.2 CALIBRATION DRIVER FUNCTIONAL DESCRIPTION

The calibration driver used in the GDAS amplifier filter deck is similar to the calibration receiver used in the J-box. Both units are comprised of the same active elements in identical circuits. The front end is a Burr Brown 3626 op-amp coupled with a Burr Brown 3329 power booster making an extremely accurate trouble free circuit, capable of driving the capacitive load of a long line with high current reserve. For further information on this circuitry refer to paragraph 4.6.2. See Figure 17 for the schematic of this circuit.

The calibration driver differs in its inclusion of an input selector switch, local input capability, and output terminal post. The selector switch has three positions, "D/A", "OFF", and "LOCAL". In the "D/A" position the input is selected from the filter deck rear panel

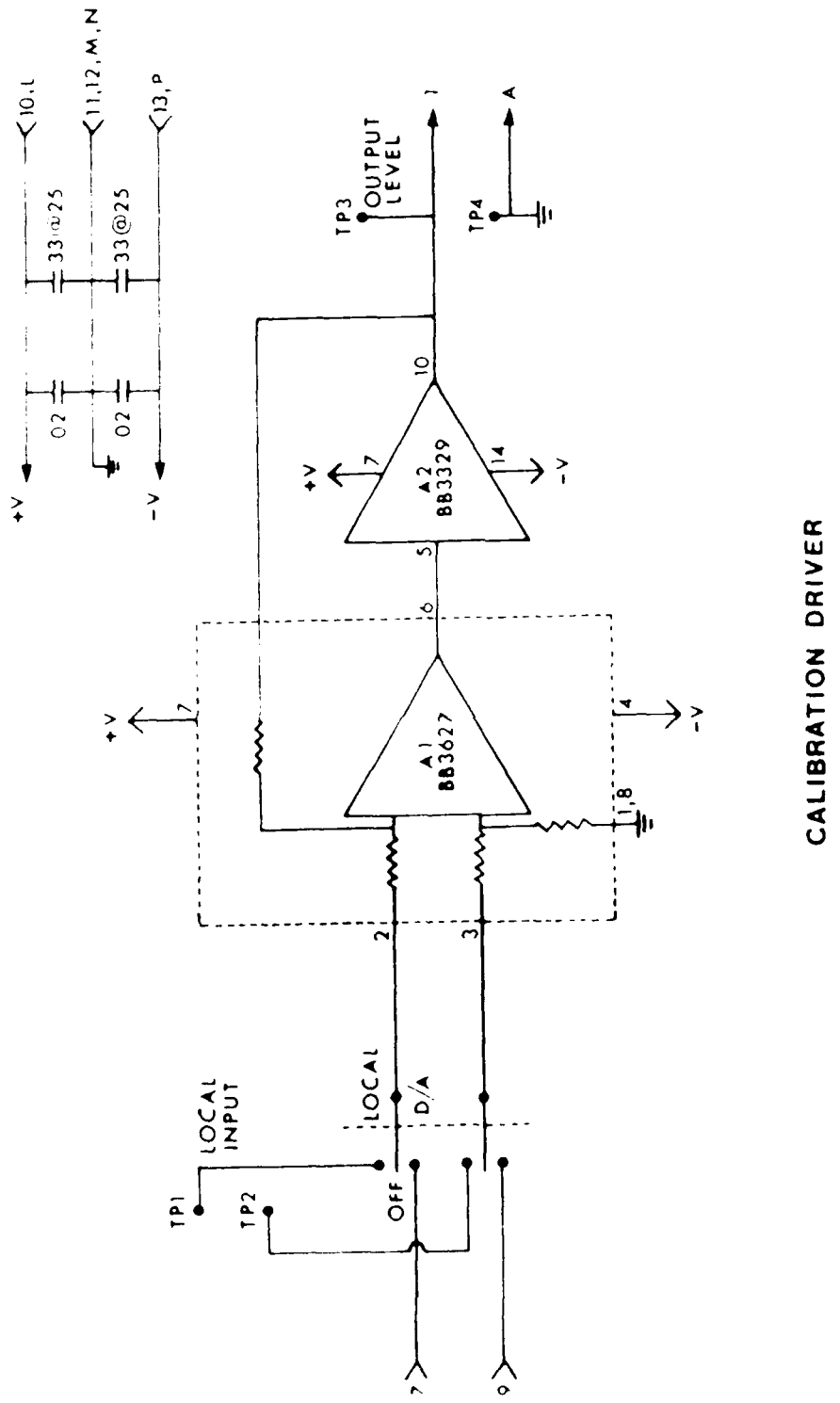


FIGURE 17 CALIBRATION DRIVER SCHEMATIC

input, normally connected to the computer operated digital to analog converter. The "OFF" position does not select an input and components force the circuit to a zero output. In the "LOCAL" position the front panel "LOCAL" test points are selected as an input. This allows full adaptability of the circuit for calibration, testing, or trouble shooting.

5.4.4 OPERATION OF SYSTEM CALIBRATOR

Refering to Figure 18, in system calibration the computer D.A.C. is the normal input providing software controlled signal, i.e., a step or time variable function. For testing purposes, or in the absence of a D/A the "LOCAL" input is used. Whatever the derivation of the signal, it is conditioned by the calibration amplifier and routed through the switch box, down the interconnecting cables to the J-boxes where it is reconditioned by an identical amplifier in the calibration receiver. The output of this amplifier is bus connected to the 17 slots in the box plus the calibration output connector.

In a seismic channel this calibration signal is sensed as a precision voltage by the calibration on the preamp card, converted to a precision current and injected into the calibration coil of the seismometer producing a known offset of the mass (motor constant). The voltage produced by the motion is sensed by the preamp and processed as a signal.

In the instance of a bridge type sensor, the calibration voltage is sensed by the voltage comparator mounted on the preamp board. If this is a positive voltage and of a greater magnitude than the trip point, the op amp will reverse polarity and close a relay in the transducer preamp, placing a precision resistor across one leg of the bridge. This known unbalance will produce a voltage offset related to the scale factor which will be sensed as a signal and processed.

The ability to test or calibrate portions of the electronic circuitry were worked into the system. The calibration output connector on the J-box can be used to monitor or verify the accuracy of the calibration signal delivers. With the properly wired connectors (deemed the "Milking Machine") the sensor must be uncoupled and the calibration signal simultaneously impressed on any or all channels, verifying gain, polarity, frequency response, etc., of the entire GDAS.

As a further aid, a prewired "Self Test" adapter can be inserted into the input connector of the signal conditioning filter deck. Again, the calibration signal is simultaneously applied to the 16 filter channels allowing, among other conditions, verification of the board as set up by the CAD programs.

5.5 AMPLIFIER/FILTER SOFTWARE

5.5.1 SOFTWARE OVERVIEW

This section briefly describes the design software developed for the GDAS. It is not within the scope of this section to produce a detailed listing of the programming. For a fuller description including the basic use and algorithms of the system definition programs, refer to references (Von Glahn, 1980; Center, 1989).

5.5.2 DESIGN SOFTWARE

Several C.A.D. programs have been developed to aid in the design of the signal conditioning filter board and the defining of the entire analog measurement system.

ACCURRACIES		
	D/A	012
	DRIVER	01
	RECEIVERS	01
	TOTAL Σ	0185

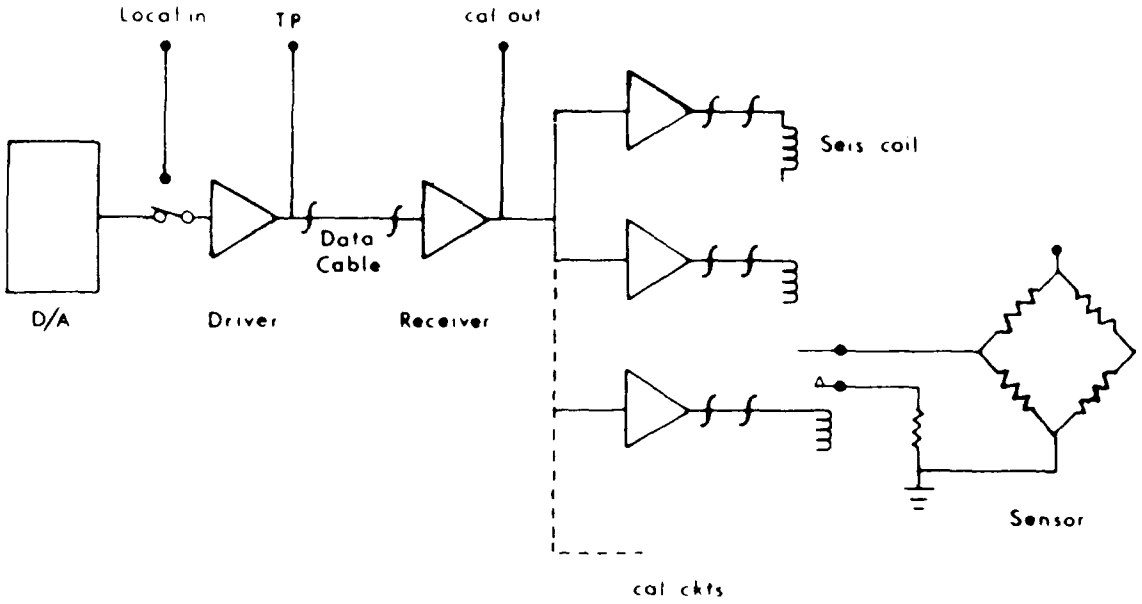


FIGURE 18 CALIBRATION CIRCUIT BLOCK DIAGRAM

5.5.2.1 AMPLIFIER/FILTER DESIGN

GKCARD is the filter circuit design program. It has evolved, from its predecessors, to the present user-friendly, interactive program with many default parameters. Its intent is to reduce the complexity of designing the Bi-Quad filter to simple inputs of required parameters. The three Bi-Quad stages are being utilized as a six pole anti-aliassing filter, with a high gain front end, stage 1.

GKCARD allows the operator to create a *.RES file, used throughout the data reduction, and will design any one or all of the stages. On calling the program, the operator is requested to name the output file, either creating it, or open an existing one. The program then presents its opening menu options.

Stage 1 update
Stage 2 update
Stage 3 update
Stage 4 update
Stage 5 update
Stage 1-5 update
Channel to channel copy
Rename Filter Card Number
Printout
Quit

After completing an option (except Quit) the user is returned to this menu. The design criteria will allow the input to be in the desired parameters, by input or default, and will return idealized, non-standard, component values. The operator must then enter the closest standard value component allowing the computer to recalculate the parameters. This process can be repeated until the desired parameters are obtained. At the completion of the design procedure a table of components and filter parameters may be output (option: Printout) to aid in the physical building of the board or for future reference.

5.5.2.2 SENSOR ENTRY

GKMAIN allows the sensor and preamp parameters to be entered into the file created by GKCARD, or will allow changes to be made to the existing file. The program assumes the *.RES file exists. Its opening menu lists the options available.

Print data file
Update sensor and/or preamp
Help
Quit

Entry of sensor parameters determine, by unit name, the type of sensor, either seismic or pressure. Preamp parameters are fixed and entered as such. The PRINT DATA FILE option will output the entire system specifications. The HELP option briefly describes the order of programs and their use to obtain the desired objective, the system transfer function.

5.5.2.3 CALIBRATION

Data obtained from the system calibration program GDASXM is combined with sensor calibration, ie. weight lifts for seismic; manometer pressure tests for pressure in programs GKCALI and GKSENS for seismic or GKGAIN and GKPOLE for pressure.

GKCALI models the seismic calibration pulse to an ideal response and requires the input of the weight lift results and calibration current facotr of the pre amp card. The results are entered into the *.RES file manually by GKSENS.

In the case of pressure transducers, the system gain is determined in GKGAIN. The hi-pass pole (time constraint of the bleeder tube used to negate long term barometric input) is determined in GKPOLE. These resutls are entered into the *.RES file via GKMAIN.

5.5.2.4 SYSTEM TRANSFER FUNCTION

Program GKTRAN primarliy produces the system transfer function from sequential execution of the preceeding programs. The results are output as a *.TRF file for future use. Options within this program allow for the printout of a table of frequency, magnitude, and phase or a plot of the system response, (a graph of output vs. frequency).

6.0 SYSTEM CONTROLLER SUBSYSTEM

6.1 CHAPTER OVERVIEW

This chapter addresses the system controller. Included is an overview of the subsystem functions and detailed descriptions of its components. Separate subsections will cover the controller chassis and wiring and the system control computer. DEC's Microcomputer Processor Handbook, 1985 offers detailed information on the system computer as well as an overview of the system software.

6.2 SYSTEM CONTROLLER FUNCTIONAL DESCRIPTION

The system controller is the heart of GDAS. It contains the digital computer that controls the recording of data and analyzes pre-recorded data. The computer also runs programs to design the signal conditioning cards, as documented in Chapter 5 of this report.

6.3 SYSTEM CONTROLLER CHASSIS DESCRIPTION

6.3.1 CHASSIS PHYSICAL DESCRIPTION

A custom-built aluminum chassis has been built to house the system controller and is designed to fit into a standard 19 in. equipment rack. Its front panel, on which is glued an engraved blue plastic dress plate is made from 0.125 in. aluminum and measures 10.48 x 19 in. A 8.5 x 11.5 in. door is cut into the front panel to allow access to the computer cards.

The chassis box itself is made from aluminum and measures 19 in. deep, 10 in. high, and 17 in. wide. It has a removable top panel to allow access to the internal components. A 0.125 in. rear panel contains engraved labels for the components mounted on it. In the middle of the panel is a grill for exhausting ventilation air. For pictorial location of component parts refer to Von Glahn (1980).

Mounted on the front panel are several switches and pilot lights. Switch S1 controls the ac power to the controller. The nearby indicator light (L1) gives a visual indication when the ac power is on. A second switch (S2) controls the dc power supplies' outputs; pilot light L2 lights up when the dc power is on. The other two switches control the status of the system computer. The RUN/HALT switch (S3) enables or disables the computer RUN mode. When the computer is running, pilot lamp L3 is on. Momentary contact switch S4 initializes (restarts) the computer. Two ventilation fans (B1 and B2) are mounted on the right side of the chassis to provide ventilation air; they are active whenever ac power in the chassis is on.

On the rear panel are mounted the input, output, and power connectors as well as a fuse. J3 through J6 provide the parallel digital connections between the interface subsystem and the parallel input/output cards mounted in the computer card rack. Connectors J7 and J8 are spare input/output connectors; they are connected to ribbon cables that run to the front of the computer card rack but which are not currently connected to any input/output cards. J11 is used to connect the winchester disk unit to its controller card. J12 is used for connecting the floppy disk subsystem to its controller card. Serial digital communications are provided through J15, J16, and J17. These are used for communications between the computer and the system console and printer. Line voltage is

supplied to the controller through J2. Two fuses (F1 and F2) provide protection for the entire controller and for the power controller card, respectively.

Card racks (BP1 and BP2) which houses the computer and interface cards,dominates the interior of the chassis. Two power supplies, PS1 and PS2, provide 12 and 5 Vdc power, respectively, for the system computer and interface circuitry. On the bottom of the chassis is mounted a power transformer (T1) which supplies low voltage ac to the power control board. This board is connected to the chassis wiring harness through edge connector J18. A ribbon cable runs from this connector to a plug (P1), which is plugged into the lower computer card cage (BP2) to provide power status signals to the computer. On the side panel of the chassis near the control board are mounted the 110 Vac control relay (K1) and an ac distribution terminal strip (TB1). Finally, a terminal strip (TB2) is mounted on the rear panel near J6 for connecting two signals, sample rate input,from this connector to J18.

6.3.2 MODIFICATIONS TO THE SYSTEM CONTROLLER

An early study of noise within the GDAS indicated a wiring problem within the system controller. Power regulation was poor and noise measurements were larger than specifications or expected level consistent with the use of switching power supplies. It must be noted that switching power supplies are generally accepted to be noisier (radiative and conductive) and less regulated than linear power supplies. This noise, predominantly high frequency current spikes, was wired to the load over tightly twisted pairs that produced an unacceptable measure of inductance (est. at 1.2 uH/foot with tight coupling for mutual inductance). The resultant voltage noise, built up over the inductances appeared at the load (the computer backplane) and contributed to an unacceptable digital noise level in the A-D converter. To further irritate this problem, no decoupling capacitors were used at the point of load and multiground routes abounded in the wiring scheme. The DC impedance of the current meters used to monitor the supply current, plus the wiring complexity to and from the meters degraded the regulation.

The two meters were deleted as unnecessary. Wiring twists were eliminated on the heavy 12 gage line and reduced on the lighter lines. Decoupling capacitors, tantalum for low frequency, ceramic for high, were mounted on the back plane. The wiring scheme was changed using a single point ground.

The chassis was disassembled, modified for better ground conduction and reassembled to allow easier access to the component parts. The computer backplane cages were moved to take better advantage of the cooling fans.

Connectors and meters that had been mounted on the rear panel and made surplus by modifications were removed. Connectors J9 through J12 were deleted or changed to the proper connector for new peripherals.

6.3.3 CHASSIS WIRING DESCRIPTION

Figure 19 shows the power and control signal wiring diagram for the modified system controller chassis. Wire sizes are annotated on the figure where they are important (to reduce voltage drop). All 110 Vac power lines are twisted as shown and routed well away from all dc and signal line.

Pin 18 on J18 is not connected to anything on the power control board. Rather, it serves as a junction point between the ribbon cable connected to P1 and the twisted pair connected to TB2, delivering the sample rate input to the BEVENT line.

Specifications for the controller power supplies are given in Table 11.

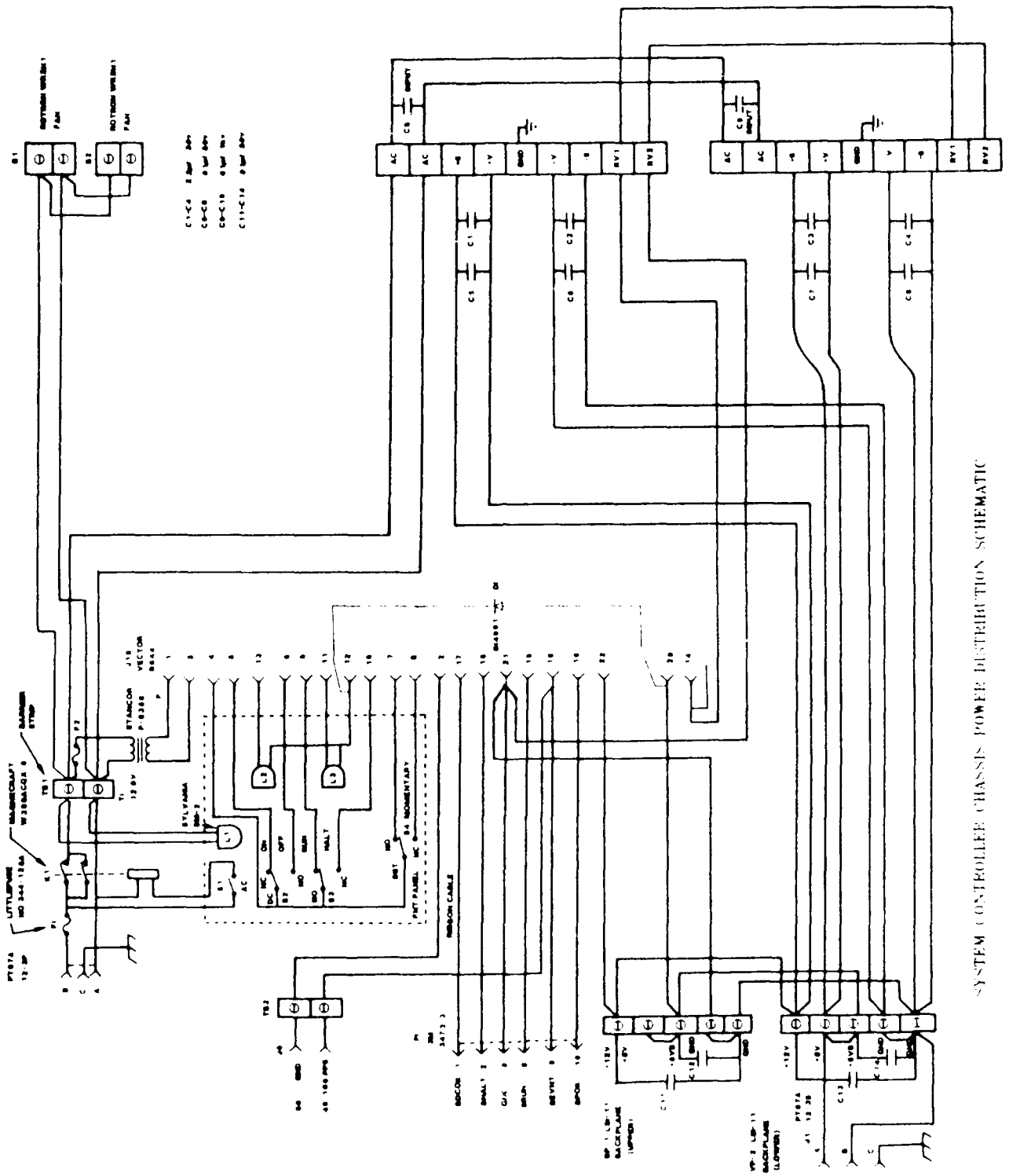


FIGURE 19 CONTROLLER CHASSIS WIRING DIAGRAM

Table 11 SYSTEM CONTROLLER POWER SUPPLY SPECIFICATIONS

5 Volt Supply:

Output Voltage	5 Vdc (± 0.25 V adj range)
Output Ripple	50 mV P-P, max
Output Regulation	± 20 mV (± 10% line, no load to full load
Output Tempco	0.03%/°C, max
Output Current	30 A at 50°C ambient 24 A at 60°C, ambient 16.5 A at 71°C, ambient
Overvoltage Protection	Built-in, 6.4-6.8 Vdc trip
Current Limiting	Built-in
Size:	6.2 x 4.7 x 10.2 in. (15.8 x 12.0 x 26.0 cm)
Operating Temperature	0° to +71°C

12 Volt Supply:

Output Voltage	12 Vdc (± 0.60 V adj range)
Output Ripple	100 mV P-P, max
Output Regulation	± 48 mV (± 10% line, no load to full load)
Output Tempco	0.03%/°C, max)
Output Current	4.2 A at 50°C, ambient 3.4 A at 60°C, ambient 2.3 A at 71°C, ambient
Overvoltage Protection	Built-in, 13.3-14.1 Vdc trip
Current Limitng	2.1 x 4.7 x 10.2 in.
Size	(5.2 x 12.0 x 26.0 cm)
Operating Temperature	0 to +71°C

6.3.4 PARALLEL INTERFACE SIGNAL WIRING

The following information pertains to connectors J3-J11 on the system controller rear panel when used with Digital Equipment Co. (DEC) DRV-11 parallel interfaces.

J3 through J11 consists of 50-pin ribbon cable connectors. Attached to these is a 50 conductor ribbon cable. Since the DEC parallel interfaces accept 40-pin ribbon connectors, the wires connected to pins 41 through 50 of J3-J11 are not used for signals but are available for other uses. The 50-wire ribbon cable is therefore split, with wires 41 through 50 tied off. The other 40 wires are terminated with a 40 place IDC plug for connection to the parallel line interface. Pin 1 of the two connectors must be connected to the same edge of the ribbon cable. A full listing of signal connections can be obtained from reference 1 or the appropriate manufacturer's manual.

6.3.5 SERIAL INTERFACE SIGNAL WIRING

Connectors J15-J17 provide null-modem RS232 connections to various serial interfaces. J15 and J16 are wired to a 40 pin ribbon connector which mates with DEC

DLV 11 interface. These two cable-connector sets are identical. J15 mated the system console to its interface. J16 was originally installed for use with a line printer. This piece of equipment is rarely used and the connector is considered as spare.

J17 is wired to a 10 pin ribbon connector an allows for the use of the system console with a DEC DLV 11J interface. Table 12 lists the interconnection between the RS232 (standard 25 place "D" connection) and the 40 place ribbon connector. Also shown in the table are the signal names.

Again, a standard wired RS232 console can be directly attached to the system controller without the need of a null module.

Table 12 RS 232 INTERFACE CABLING

RS 232				
1		Protective Ground		A
		Protective Ground		VV
2		Transmitted data		J
3		Received data		F
4		Signal Ground		B
7		Signal Ground		UU
20		Data Set Ready		Z
				E
				M

DLV - 11 connections

RS 232				
1		Protective ground		
2		Transmitted data		3
3		Received data		8
5				
6	750Ω	DTR		10
7		Signal Ground		2
8				

All components for the power control circuits are mounted on a single 4.5 x 6.5 in. double-sided printed circuit board. Signal and power connections to the board are made through a 44-pin edge connector.

6.3.6 POWER CONTROL CIRCUIT DESCRIPTION

This section covers the circuitry needed to provide power status and control signals for the system control computer and power supplies. These signals meet the timing requirements specified by DEC. All circuitry, excluding switches and indicator lamps, is mounted on a single printed circuit board. The following sections document the circuit functions and schematics.

All components for the power control circuits are mounted on a single 4.5 x 6.5 in, double-sided printed circuit board. Signal and power connections to the board are made through a 44-pin edge connector.

6.3.6.1 CIRCUIT BLOCK DIAGRAM

Figure J-1, (Von Glahn, 1980),shows a block diagram of the power control board. As shown on the diagram, the circuit has its own power supply for running the on board logic. The ac is also fed into a sensing circuit as are the leads from the DC ON/OFF front panel switch. This circuit generates ACON when the power is present and DC ON/OFF switch is on. This signal is delayed and provides the control signal to turn on the controller power supplies.

The outputs from the controller power supplies are fed to the dc sensing circuit. This circuit generates DCON when both supplies are at operating level (over 90% of final value) and turns on the DC on pilot lamp. The ACON, DCON, and the signal from the momentary "INIT" switch are presented to a delay and logic circuit. It in turn provides the properly-timed status signal, DCOK and POK, to the system computer for both power up and power down conditions.

A buffer on the board converts the output of the "RUN/HALT" front panel switch to the HALT signal for the computer.

The SRUN signal from the computer is fed to a retriggerable oneshot multivibrator on the board. SRUN consists of a pulse train that is present when the computer is running. The oneshot output drives the RUN lamp on the front panel.

Finally, one pin on the board edge connector is used as a junction point. Connected to it is the time variable pulse train from the system clock being fed to the BEVNT line in the computer, and is used as the sampling interupt for the system.

6.3.6.2 CIRCUIT TIMING INFORMATION

Figure J-2 (Von Glahn, 1980), is a timing diagram for key signals on the control card. As shown in the figure, turning on system power (via the ac ON/OFF switch) is a prerequisite for circuit operation. When the dc ON/OFF switch is thrown, the ACON signal goes high, indicating the presence of ac power and initiating the power up timing sequence. This signal is delayed by 5.5 msec to provide the control signal for the chassis power supplies. When the slowest of the two supplies reaches 90% of full scale output, the DCON signal goes high. This signal is delayed by 3.6 msec and becomes the DCOK signal for the computer. A further 97 msec delay results in the POK signal, which is also sent to the computer.

The power down timing sequence begins with either a shut off or failure of ac power or throwing of the dc ON/OFF switch. Either action results in the negation of the ACON signal. Following a 5.2 msec delay from this negation, both the power supply control signal and the POK are negated. After a further 4.8 msec delay, the DCOK signal is negated and the power down sequence is completed.

6.3.6.3 POWER CONTROL CIRCUIT SCHEMATIC

The schematic for the power control card is shown in Figure J-3 (Von Glahn, 1980), Relating the schematic to the block diagram, diodes CR1-CR4 together with capacitor C1 and voltage regulator U1 make up the onboard 5 Vdc power supply. Note that an external diode must be mounted between the output of this supply (at pin 12 on the edge connector) and the +5 V input to the dc sense circuit (pin 20). This diode allows the chassis power supply to power the circuit card after ac power fails. Since the chassis power supply has a longer decay time than the onboard supply, this connection insures orderly power-down timing.

Zener diode VR1 along with R1-R3, C2, and Q3 convert the incoming 12.6 Vac power to 5 Vdc power and a 5 V pulse train for the ac sense circuit. The sense circuit is made up of a dual monostable multivibrator (U2) and associated components. The monostables have pulse widths of approximately 10 msec. They are triggered by opposite rising edges of the pulse train from Q3. Both mono stables are either enabled or disabled by the dc ON/OFF switch which is debounced by two sections of a hex inverter, U7. When enabled, the two pulse train are combined by an OR gate (U3) to form the ACON signal. This signal is buffered by an open collector NAND gate (U5) and fed to an RC timing circuit made up of R9 and C5. The voltage across C5 is compared to a reference by comparator U6. When the voltage exceeds the threshold, U6 trips and generates the control signal for the chassis power supplies, DCONC. DCONC is also inverted by U5 to allow control of power supplies requiring the opposite polarity signal. A jumper allow selection of control signal polarity.

Comparators U9 and R15-R22 make up the dc sense circuit. The two power supply outputs are connected to resistive dividers. The outputs of these two dividers are compared to a reference voltage (generated by R19 and R20 from the +5 V power line) by the comparators. The comparators outputs are combined by U8 to yield the DCON signal. This signal feeds the dc lamp driver made up of a R32 and Q2.

Comparators U10 and associated components, as well as gates U8 and U3 make up the logic and delay circuits that generate the DCOK and POK signals for the computer. As for the DCONC signal, delays are generated through RC delays feeding the two comparators. C11 and C12 on the two comparators provide positive feedback to insure clean switching of the comparators' outputs.

Two sections of hex inverter U7 and one section of an open collector NAND gate (U5) buffer the RUN/HALT switch output. The resulting signal feeds the BHALT signal to the system computer.

A retriggerable monostable multivibrator (U4 provides the pulse to level conversion for the RUN lamp driver made up of R8 and Q1. The monostable pulse width of 80 msec is considerably wider than the SRUN signal period so the monostable is continually retriggered as long as SRUN is present.

6.4 SYSTEM CONTROLLER COMPUTER DESCRIPTION

6.4.1 CHAPTER OVERVIEW

This chapter presents information on the system controller. It offers a brief description of the components including modifications and necessary jumpers for standardized addressing. It also defines a minimal system, the card cage priority assignments and a system memory map.

The information included herein is not meant to be all-inclusive; rather it is designed to provide sufficient detail to allow the system user to correctly configure a minimum GDAS without reference to other documents. For those requiring more detailed

information on the LSI-11 family of modules and backplanes, the appropriate DEC or manufacturer's manual is recommended.

6.4.2 GENERAL DESCRIPTION

Acting as the controller for all digital data acquisition and analysis functions, the system computer can be considered the heart of GDAS. It consists of a DEC LSI 11/23 microcomputer, a number of interface cards, and memory. The computer is housed in a card rack in the controller chassis and can be accessed through the front panel door of the chassis. The rack itself consists of card guides and a backplane/socket array into which the computer cards are plugged. The computer communicates with the outside world through interface cards which are connected to the chassis back panel by multiple-conductor ribbon cables as discussed in the previous section. The following sections describe briefly the system computer components.

6.4.3 CARD CAGE AND BACKPLANE DESCRIPTION

All LSI-11 system circuit boards are housed in two DEC H9270 backplane/ card cage assemblies. These are mounted in a custom-built aluminum rack in the controller chassis. Room has been left in the rack for a third backplane assembly should further expansion require it. The two backplane assemblies are jumpered together using wire wrap techniques. Table 13 indicates the jumpered pins. The units use the Q bus technology developed by DEC.

DEC's LSI computer and support circuitry are mounted on printed circuit boards of two sizes: dual, and quad height modules. These backplanes provide enough room for the LSI 11/23 processor and up to 7 quad-height or 15 dual-height modules or any combination thereof. The backplane provides power and most of the signal interconnections between the modules.

6.4.4 BACKPLANE INTERRUPT PRIORITY ASSIGNMENT

The LSI computer system uses a daisy-chain, 'Z' fold, interrupt priority system. Interrupt priority assigned to a given module is determined by its position in the chain. Those modules that are electrically closer on the chain to the computer will have a higher priority. Priority assignment is determined, then, by the position of the module in the backplane. Figure 20 shows the priority structure of the double-backplane card cage used in the GDAS. It represents a view of the cage looking through the controller chassis access door. (The cards are oriented horizontally, component side down; each rectangle is a double-height module.)

Table 13 BACKPLANE JUMPER LIST

AA1	AJ1	AT1	BF2	BP1
AB1	AJ2	AT2	BH2	BP2
AB2	AK2	AU2	BJ2	BR1
AC1	AL2	AV2	BK2	BR2
AD1	AN1	BA1	BL2	BS2
AE2	AP1	BB1	BM2	BT2
AF2	AP2	BB2	BN1	BU2
AH2	AR1	BE2	BN2	BV2

CPU backplane AN2 - second backplane AM2
CPU backplane AS2 - second backplane AR2
CPU backplane CH1 - second backplane AF1

Note: Jumpers are between the two card cages ie; AA1 backplane is jumpered to AA1 backplane 2 etc.

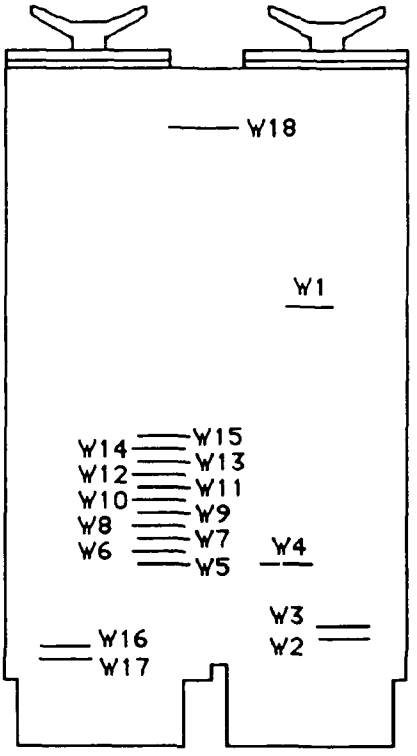
14	PRIORITY 14
13	12
10	11
9	8
6	7
5	4
2	3
PRIORITY 1	LSI 11/23

FIGURE 20 SYSTEM CONTROLLER COMPUTER BACKPLANE INTERRUPT PRIORITY ASSIGNMENT.

6.4.5 MICROCOMPUTER DESCRIPTION

A DEC LSI - 11/23, a 16 bit machine, has replaced the LSI-11 as the system microcomputer. This unit is built on a standard dual-height board and is considered "upward compatible" from the LSI-11. Specifically the module is identified by the number M8186 and is a model number KDF11-AA.

The LSI - 11/23 boasts 2.5 times the speed of its predecessor. It is complete with a floating point instruction set and a memory management unit which allows addressing of up to 256K bytes of main memory. Figure 21 shows the jumpers necessary for operation within the present GDAS. The use or name of these jumpers plus a fuller description of the microcomputer are contained in the DEC Microcomputer Products Handbook 1985.



Jumper	Configuration
W1	I Do Not Remove
W2	Fixed
W3	Fixed
W4	R
W5	R
W6	I
W7	R
W8	I
W9	I
W10	I
W11	I
W12	I
W13	I
W14	I
W15	I
W16	I Do not Remove
W17	I Do Not Remove
W18	R

I = Installed
R = Removed

FIGURE 21 MICROCOMPUTER JUMPERS

6.4.6 MAIN MEMORY DESCRIPTION

The memory modules presently used with the GDAS are manufactured by PEBX Inc. model MEccV11-L. This system is contained on two dual-height cards, one a controller the other containing the memory chips, placed in adjacent Q bus slots and connected with a 50 pin flat ribbon cable.

The system is a 256K byte self-correcting MOS parity memory. Refresh, accomplished without computer interruption, is derived from BDCOK. Operation is transparent to the programmer/user. Operation power is obtained from the bus. This unit is similar to the DEC MSV11 memory set and will execute the MXV11 diagnostics.

6.4.7 INTERFACE MODULE DESCRIPTION

The interface modules permit the computer to communicate with the outside world and transfer the data to/from various mass storage units and/or memory. Some of the peripheral equipment used with the GDAS is supplied with its own dedicated interface, and as such their description including strapping is included in the operation manuals of the equipment.

DEC interfaces used in the GDAS are one of two types, serial or parallel. The following sections give a brief description of these units. Jumpering of the various interfaces (address, vector, mode of use) will be covered in the section devoted to the equipment they are used with.

6.4.7.1 DLV-11 Serial Interface

DEC DLV-11 asynchronous serial interface (module M7940) is used in the GDAS for communications with the system consile under RS 232 format. The dual height cord can be configured for various baud rate and operates as a full duplex serial link. Signals to and from the unit are through a ribbon cable socket on the board.

6.4.7.2 DLV-11E Line Interface

The DLV-11E asynchronous serial interface is primarily intended for modem contol under RS 232 format and can be configured for various baud rates and operating parameters.

6.4.7.3 DLV-11J Four Channel Serial Interface

The DLV-11J is a four channel asynchronous serial interface, which operates on a limited number of address/vectors. It's operation is, for GDAS functions, four DLV11's on one dual board, and will service the system console and any of several asychronous serial units, ie. a printer.

6.4.7.4 DRV-11 Parallel Interface

For parallel interfaces, the GDAS uses the DEC's DRV-11 parallel line units (module M7941). They provide 16 input, 16 output, and 4 control lines between the module and the device connected to it. All lines are TTL level and appear on two ribbon cable sockets on the board. The module is dual height.

6.4.7.5 DRV-11 B Parallel Interface

The MDB DRV-11 B is a direct memory access (DMA) parallel interface used in controlling the operation of data transfer from the Preston A/D converter. Control and status is interactive with the processor. Data transfer, in random length blocks of 16 bit words, is done without intervention of or interruption by the processor (principle of DMA). All transfers are via the"Q" Bus and software supports data transfer to any mass storage device on line in the GDAS.

The interface is a quad height card and resides in the controller backplane. Communication and data transfer to and from the Preston is over two 40 conductor flat ribbon cables. Control of the interface by the processor is via the bus.

6.4.8 ADAC 1200 CONTROLLER

A second controller had been added to the GDAS mainly to increase the number of units available. When in use, the GDAS is dubbed "GDAS Peculiar."

Two modifications must be made to allow its inclusion. First and foremost is the removal of the ±15 volt power from the backplane as ADAC uses DEC prepriotory lines for this use. Even with this deletion certain equipments may not operate properly in the controller.

The real time clock (DEC BEVENT) center jumper must be wired to a user installed BNC connector. Properly labeled "Sample Rate Input", this connector is jumpered to a modified Interface Subsystem Box connector labeled "Sample Rate Output".

The use of a bootstrap procedure without a BEVENT mask will require manual setting of the RTC front panel switch.

With these modifications and precautions the unit is user transparent in all areas except a local bootstrap "INIT" switch. For a complete description refer to the ADAC 1000 instruction book.

7.0 INTERFACE SUBSYSTEM

7.1 CHAPTER OVERVIEW

This chapter covers the interface subsystem, the system digital clock, and the system digital tape recorder. It includes an overview of the subsystems and their interrelationships. Separate sections then cover the interface chassis and its wiring, the system clock and its interface, and the system digital tape recorder and its interface. Detailed support information is included as required in each section.

7.2 INTERFACE SUBSYSTEM FUNCTIONAL DESCRIPTION

The interface subsystem houses interface circuits to interconnect the computer's parallel ports with the system clock and digital tape recorder.

Mounted in the interface chassis is the system clock. The clock provides the calendar date and time for data identification as well as timing pulses to initiate data sampling. These signals are routed through the interface electronics to the computer.

The system digital tape recorder provides bulk storage on magnetic tape of data acquired by the GDAS. It also can play back prerecorded data tapes for analysis. Input and output signals to/from the recorder are routed through the interface electronics to/from the computer.

This system has been modified to contain its own power supply, and a sample rate output allowing the use of the ADAC mainframe in the GDAS.

7.3 INTERFACE CHASSIS DESCRIPTION

7.3.1 PHYSICAL DESCRIPTION

A custom-built aluminum chassis houses the interface hardware and is designed to fit into a standard 19 in. equipment rack. Its front panel is covered with a blue plastic dress panel and measures 6.96 in. Also mounted on the panel is the system clock. A 5 x 8.25 in. bottom-hinged door is cut into the panel to allow access to the interface cards.

The chassis sides, top, and bottom are made from aluminum and measure 19 in. deep, 6.5 in. high, and 17 in. wide. The chassis has a removable top panel to allow access to the wiring and card cage. A rear panel contains cutouts for a ventilation fan and for assorted power and signal connectors. Engraved labels are provided on the panel for ease of system interconnection.

The chassis is mounted in the equipment rack on two chassis slides , one on each side of the unit. A ventilation fan (B1) mounted on the rear panel provides ventilation for the components inside; a grill in the chassis top allows the air to exhaust. All input, output, and power connectors are mounted on the rear panel. AC power for the fan and clock and power supply is supplied through J1. A fuse (F1) provides protection for this power. Sockets J3 through J9 connect the interface cards to the parallel interfaces in the controller subsystem. Two BNC connectors (J10 and J11) provide an external connection point for access to the clock master oscillator for special applications. For normal GDAS operation, a BNC to BNC jumper is installed between the two connectors. A third BNC connector provides a "Sample Rate Output" from the system clock. Finally, J12 and J13 connect the interface cards to the system tape recorder.

An internal card cage is made from a modified commercial card guides and edge connectors mounted between two custom-made aluminum plates. The system clock is inserted through the front panel and is supported by an aluminum bracket.

7.3.2 CHASSIS WIRING

Power and ground lines are bussed between the edge connectors. Wirewrap jumpers are used between the two tape recorder interface card connectors. Although the card cage has slots for six circuit boards, only four circuit board edge connectors are currently installed (three active and one spare).

Connections between the card edge connectors and sockets J6-J9 on the back panel are made using 50-conductor ribbon cable. (Sockets J3-J6 are spares and are plugged with ribbon cable connectors to keep out foreign objects.) The back panel end of the cable is terminated with a 50 place IDC socket; the other end terminates with a 50 place connector that plugs directly onto the card cage edge connector pins 1-50. A keying reader on the connector pins insures proper alignment.

Connections to the on card sockets are also made using ribbon cables. A 50-conductor cable connects the clock interface to the clock. Forty-conductor twisted pair cables are used to connect the tape recorder interface cards to J12 and J13 on the back panel.

Single conductor coax cable connects the clock interface edge connector with J10 and J11. The edge connector end is stripped and soldered to the edge connector pins, while the other end is terminated with a BNC male connector.

7.4 SYSTEM CLOCK AND CLOCK INTERFACE

7.4.1 CLOCK DESCRIPTION

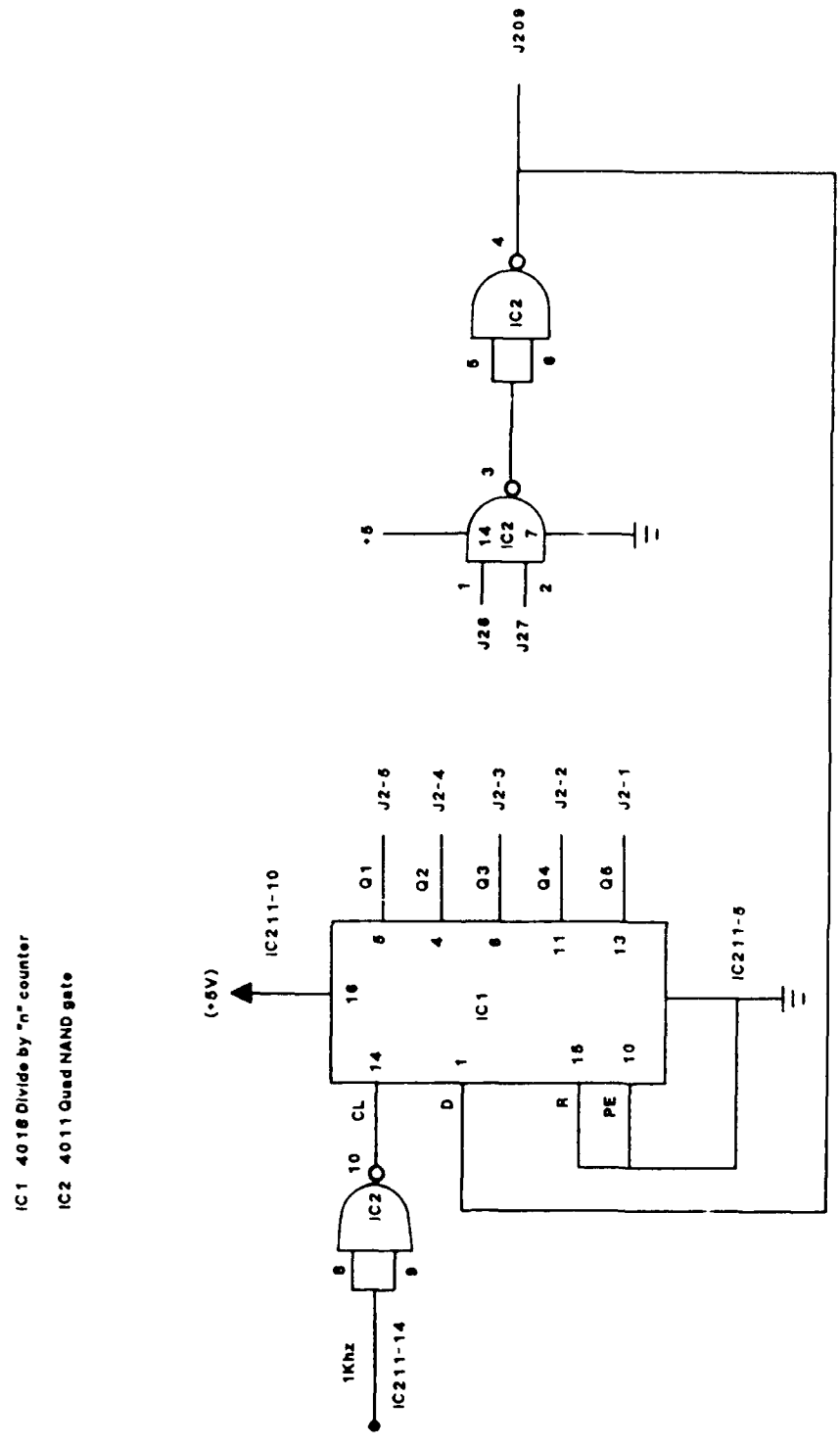
The system clock serves two main functions: providing date/time information for recording on the data tapes, and providing the master timing source for data acquisition.

An Electronic Research Company (ERC) model 2446 digital calendar clock is used as the GDAS master clock. (Note: ERC no longer makes calendar clocks.) The clock is powered from the 110 Vac power line and uses an internal crystal time base. It provides TTL-level calendar day and time (24 hr period) information in binary coded decimal (BCD) format to the interface. Also sent to the interface is a 1 pps to provide interrupts. These interrupts can be disabled under user control (see below).

The ERC clock countdown circuitry has been modified to produce a step variable TTL signal used as a sample rate clock. The 1000hz signal supplies the input to the modification. A front panel rotary switch controls the output of the sample rate clock in sub multiples of the 1000hz, i.e. 1000/2, 1000/3 ...1000/10 producing a sample rate of 500, 333, 250, 200, 167, 143, 125, 111, or 100 SPS. Time wise this corresponds to 2, 3, 4, 5, 6, 7, 8, 9, 10 milliseconds between samples. A schematic of this modification has been added to the ERC users manual and is included as Figure 22.

On the clock's front panel are the user controls. A SET/RUN switch controls the state of the clock. When the switch is in the SET position, day and time (hours and minutes) values can be set into the clock using the pushbutton switches below the time display. When the switch is moved to RUN, the clock starts counting off time, automatically advancing the day count at 0:00:00 hours. A switch to the left of the day display provides for leap years (366 days).

Two printed circuit edge connectors on the back of the clock provide power, control, and data signal connections.



STEP VARIABLE SAMPLE RATE MODIFICATION

FIGURE 22 ERC PARALLEL LINE INTERFACE

The clock has been modified to allow external signal synchronization. The oscillator divider chain is broken at the 1000 pps level and the 1000 pps signal routed to a spare pin on the edge connector. The next divider stage input is also brought to another spare pin on the connector. These signals are buffered and routed to the chassis on the back panel.

Table 14 lists clock specifications.

Table 14 SYSTEM CLOCK SPECIFICATIONS

Time Base:	Crystal Oscillator
Worst Case Accuracy (constant temp)	± 5ppm.
Oscillator Tempco:	± 20 ppm/°C
Oscillator Frequency:	1.00 MHZ
Operating Temperature:	0 to 50°C

7.4.2 CLOCK ADAPTER DESCRIPTION

For a more detailed description, including schematics, refer to (Von Glahn, 1980). The adapter consists of a multichannel two-to-one line multiplexer to connect the 30 BCD date/time signals from the clock to the 16 parallel input lines of the LSI-11 parallel interface. Two resettable flipflops on the card buffer the one pps interrupt signal; they are cleared by control signals from the LSI-11 parallel interface card. Finally, a number of buffers are included on the card to isolate the assorted control and pulse train signals that pass between the clock and the system computer.

7.4.3 CLOCK ADAPTER BLOCK DIAGRAM

A block diagram of the clock adapter is shown in Figure K-1, (Von Glahn, 1980). The adapter consists of a 16-channel 2 to 1 multiplexer to connect the clock BCD data to the parallel input port. Buffers for the sample rate and 1000 pps bit streams are included as are buffers for the two clock control lines. Two flipflops are used to connect the 1 pps signal to the parallel port card interrupt inputs. They are reset by three signals from the computer.

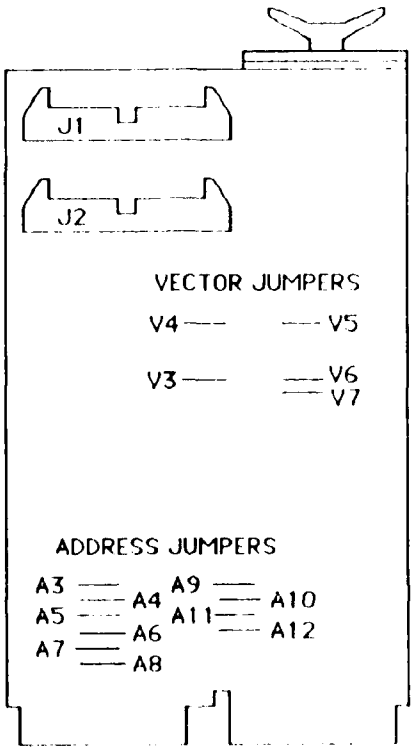
7.4.4 PHYSICAL DESCRIPTION

All components for the adapter are mounted on a single 4.5 x 6.5 in. double-sided printed circuit board. Connections between the adapter card and the clock take place over a 50-conductor ribbon cable. One end of the cable is terminated with a 50-pin plug for connecting to the card. The other cable end is split and connected to the two circuit board connectors on the back of the clock. Table K-2, Reference 1 gives the signal assignments of this cable, referenced to the ribbon cable socket on the circuit board.

Connection between the adapter card and the chassis back panel are made through the card edge connector, as are power and ground connections. The back panel connections are made via a 50-conductor ribbon cable. The card end of the cable is terminated with a 50 place socket that plugs directly onto the edge connector socket. The other end of the cable is split, with the first 40 wires terminated in a 50 place socket appearing as J7 on the chassis rear panel. The other 10 wires in the cable are soldered to a second 50 place socket on the chassis rear panel (J6).

7.4.5 ERC CLOCK PARALLEL INTERFACE

The clock interface is a DEC DRV 11 parallel line unit. The dual height board is a model #7941. The device address used is 167770, with an interrupt vector of 170. Jumper requirements are listed in Figure 23.



Jumper	Condition
A3	R
A4	R
A5	R
A6	R
A7	R
A8	R
A10	R
A11	R
A12	I
V3	R
V4	R
V5	R
V6	R
V7	I

A Address
V Vector
R Removed
I Installed

FIGURE 23 ERC PARALLEL LINE INTERFACE

8.0 SYSTEM PERIPHERALS

8.1 CHAPTER OVERVIEW

This chapter describes the peripheral hardware and their interfaces needed for GDAS operation. This hardware includes the digital tape recorder, system consoles, analog to digital computer, Winchester-floppy disk system, bubble memory, and various other "one of a kind" items that have been acquired for base station or special purpose. An in depth description can be found in the equipment users manual.

8.2 DIGITAL TAPE RECORDER AND INTERFACE

The system digital tape recorder provides a means of data storage in the GDAS. It also can be used to play back previously-recorded data tapes for analysis.

A Kennedy Corp. (Altadena, CA) model 9832 buffered digital tape transport is used as the GDAS digital recorder. It records IBM-compatible (NRZI) tapes in a 9-track format. Half-inch digital magnetic tape is used on 8.5 in. reels (1200 ft length, nominal); recording density is 800 bpi.

The built-in formatter in the recorder handles many of the functions normally performed by the user. The formatter consists of two 1024-character buffer memories and appropriate control, error check, and interface circuitry. (Character size is 8 bits for 9-track operation). The received data is loaded into a memory which, when full, is swapped with the second memory. While the second is being filled with data, the first is being recorded on tape as a 1024-character record. When the second buffer is full, it is swapped with the first and the process of loading and dumping to tape continues. Should the second memory fill before the first is finished dumping to tape, a busy signal is sent to the user until a memory is free for loading. The formatter includes built-in read after write capability to perform error checks of the recorded data. Should an error be detected, the unit automatically backspaces the tape and rerecords the data. The entire load/write process can support an average asynchronous data rate of 13,617 characters per second (maximum burst data rate is 250,000 characters per second).

For reading data, the formatter initially loads a 1024-character record of data into both buffer memories. The first buffer is then made available for asynchronous user readout. When it is empty, the second buffer is made available for user access while the first is being filled from the tape. The data is available as an 8-bit parallel word. As in read, automatic error checking and rereading is built into the formatter. In the read mode, the transport can support an average read rate of 13,617 characters per second.

Other functions are also performed by the formatter. A command allows the user to dump a partially filled memory to tape. Another command writes an end of file to the tape, while further commands control read/write status, initiate a rewind of the tape, and reinitialize the formatter.

Weighing 50 lb, the recorder is designed to mount in a standard 19 in. equipment rack occupying 12.25 in. of rack space. The unit is 16.68 in. deep and requires a 110 Vac power source. It is rated for operation over a +2 to +50°C temperature range.

8.2.1 TAPE RECORDER MODIFICATION DESCRIPTION

Operational problems (due to crosstalk between write data lines and write command lines) resulted in a redesign of the tape recorder write adapter card. This card plugs into

the rear of the recorder and connects the recorder's internal data and control signals to the outside world.

The circuitry is comprised of six dual differential line receivers . The receivers accept differential digital signals from the write interface and convert them to TTL levels for the Kennedy inputs. The response of each receiver is tailored to the timing requirements of the signal being received.

Connections between the interface card and the Kennedy recorder are made through the card edge connector. See schematic diagram for connector board, type 4463-001, in the recorder operation and maintenance manual for details on the edge connector pin identification.

One additional wire must be added to the Kennedy formatter chassis to supply power to the new write card. A wire-wrap jumper must be installed between pin 18 on the write card socket and pin D of the socket for Kennedy card 36-7-003. This card is located immediately above the write interface card in the formatter card cage. These modifications are transparent to the GDAS user.

8.2.2 RECORDER READ/WRITE ADAPTER

The read and write adapter cards, located in the interface chassis card cage, provide the digital exchange between the tape recorder and the DRV-11 parallel line interface module in the system computer. The read, write, status, and control functions performed by the adapter are split between the two cards.

Byte-parallel data for recording comes from the DRV-11 parallel interface card. The signals are conditioned on the cards and fed to the recorder in differential form. The differential line drivers on the card are connected to provide signal inversions to match the DRV-11 positive logic to the negative (low true) logic required by the recorder.

The recorder output signals also use negative logic. Therefore, the byte parallel read data and all recorder status lines are inverted to be compatible with the computer's positive logic. Also, all recorder output lines use open collector line drivers, so pullup resistor networks are used to provide proper signal termination.

Two of the status lines from the recorder are pulses as opposed to levels. To insure that the computer reads these properly, pulse-to-level conversion flipflops are used. These and other recorder status signals are combined to yield a composite error signal. This signal is fed to the computer for error interrupt and indentification purposes.

Most commands to the recorder are in the form of pulses. A pulse generator oneshot multivibrator converts a level change from the computer to a pulse. This pulse is combined with command and status bits from the DRV-11 to generate the 10 control signals for the recorder. Six of these signals are associated with writing data to tape. They are converted to differential form to match the differential line receivers added to the recorder.

8.2.2.1 READ ADAPTER CIRCUIT BOARD DESCRIPTION

All components for the adapter are mounted on a single 4.5 x 6.5 in. (11.4. x 16.5 cm) double-sided printed circuit board. Power connections to the board are made through the board's edge connector as are connections between this and the write interface card. Connections between the board and J12 on the interface chassis rear panel are also made through the edge connector. Connections between the card and the recorder read connector are made through a ribbon cable socket mounted on the card edge.

Connections between the card and the Kennedy recorder are made via J1 on the card. A 40-conductor twisted pair ribbon cable is used for the connection. A printed circuit

adapter is mounted on the chassis rear panel connector (J12) to convert the ribbon cable to the 37-pin connector used by the recorder.

8.2.2.2 WRITE APADTER CIRCUIT BOARD DESCRIPTION

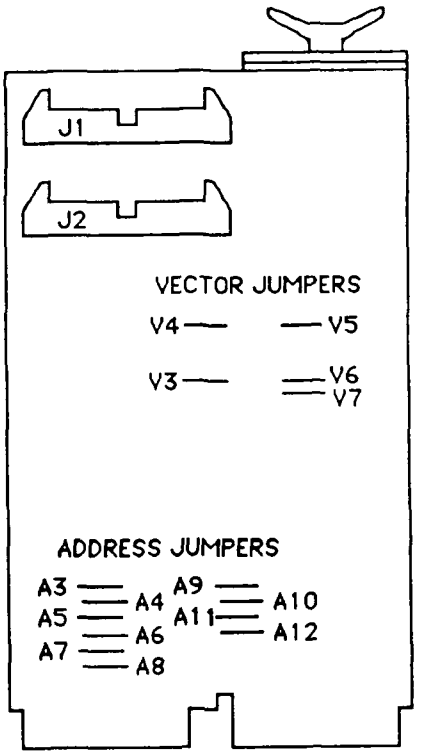
This card contains the differential line drivers for interfacing with the modified tape recorder. It also contains pull-up resistors and inverting buffers for those status signals that appear on the write connector. These status signals are routed to the read adapter. All components for the adapter are mounted on a single 4.5 x 6.5 in. double-sided printed circuit board. Power connections to the board are made through the board's edge connector as are connections between this and the read adapter card. Connections between the board and J13 on the interface chassis rear panel are also made through the edge connector. Connections between the card and the recorder write adapter card connector are made through a ribbon cable socket mounted on the card edge.

The card edge connector is used for connecting power and ground to the board as well as for connecting signals between the card and the computer parallel interface. Also run through the edge connector are signals that flow between the two adapter cards (read and write).

Connections between the card and the recorder are made via J1 on the card. A 40-conductor twisted pair ribbon cable is used for the connection. A printed circuit adapter is mounted on the chassis rear panel connector (J13) to convert the ribbon cable to the 37-pin connector used by the recorder.

8.2.3 KENNEDY RECORDER PARALLEL INTERFACE

The recorder interface is a DEC DRV-11 parallel line unit. It is a dual height board, model #7941. The device address used in GDAS is 167760, and an interrupt vector of 230. Jumpers required for this configuration are listed in Figure 24 below.



Jumpers	Condition
A3	I
A4	R
A5	R
A6	R
A7	R
A8	R
A9	R
A10	R
A11	R
A12	I
V3	R
V4	R
V5	I
V6	I
V7	I

A = Address
V = Vector
R = Removed
I = Installed

FIGURE 24 KENNEDY PARALLEL INTERFACE

8.3 SYSTEM TERMINALS

8.3.1 TEKTRONIX 4025 COMPUTER DISPLAY TERMINAL

A Tectronix Model 4025 computer display terminal is used as one of the GDAS computer system consoles. The terminal has the capability of displaying both alphanumeric and graphic data using a raster scan display format. It can display 34 lines of 80 characters of ASCII alphanumeric data stored in a built-in 16k-byte buffer memory. Up to 2048 cells of graphics can also be displayed in the user-defined graphics area (each cell is a 14x8 dot matrix). The terminal allows offline editing of text prior to transmission to the system computer. Most keys on the console keyboard can be redefined by keyboard-entered commands as can the communications interface configuration. The terminal communicates with the system computer over an RS232 serial line with data rates up to 9600 baud in a full or half duplex mode.

The detachable terminal keyboard has an 8 ft cable connecting it to the display; this allows considerable leeway in terminal installation. The display measures 12.5 x 17.5 x 21.3 in. , while the keyboard measures 3 x 18 x 9.3 in. Rated at an operating temperature range of +10 to +40°C, the terminal can be stored at -60 to +50°C. It weighs 60 lb .

8.3.2 TEKTRONIX 4105A COLOR DISPLAY TERMINAL

A Tektronix 4105A microprocessor controlled color display terminal has replaced the Tektronix 4025 terminal as the GDAS computer system console. No interface changes were required, therefore the 4025 can still be utilized for less demanding applications.

The 4105A terminal contains a 64 color palette (8 color, 8 textures) for both color graphics and text, and will run in several software plot routines including TEK PLOT 10 TCS in use with this system. The terminal is supported by both EDIT (emulates DEC VT 100) and DEC VT52, both off line screen editors. Graphics and text can be displayed on the screen simultaneously (separate GRAPHICS and DIALOG area) and manipulated independently. In DIALOG operations 30 line of 80 characters can be displayed (12 x 6 dot matrix) with 18kB of buffered memory for scroll capability.

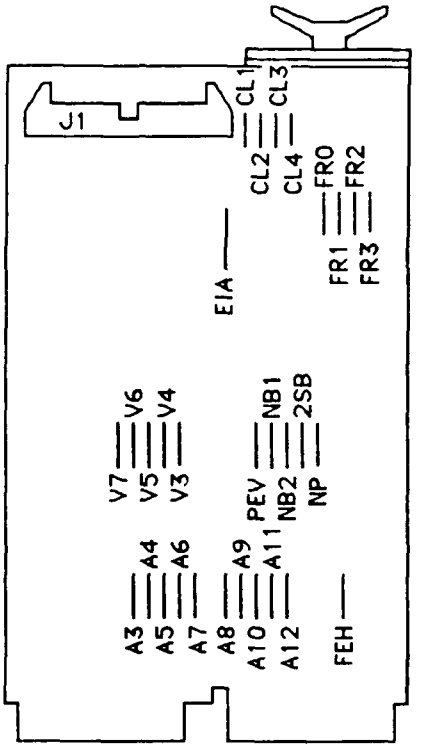
In GRAPHICS mode the system features a 480 x 360 pixel resolution on a 13 inch color display screen, with a total graphics area of 512 x 360 pixels and an addressable area of 4096 x 4096 points.

A Joystick control can be used either for scrolling in the dialog mode or as a cross hair cursor in the graphics.

The terminal features a fully removable keyboard for use adaptability which measures 16.7"L x 7.1"W x 1.6"H. The display unit measures 19.5"L x 16.5"W x 13.9"H. The two units together weigh approximately 46 lbs. The display area (13 in diagonal CRT) is 9.4 x 7.1 inches.

8.3.3 CONSOLE SERIAL INTERFACE

The interface used with the console is a DEC DLV 11 Serial Line Unit model # M7940. As used, the interface had a device address of 177560 with an interrupt vector of 060. It operates as a 9600 baud E1A device. Figure 25 shows the location and status of necessary jumpers. For a full description of the jumpers and their function, refer to the DEC Interfaces Handbook.



Jumper	Status	Jumper	Status
A3	I	PEV	R
A4	R	FEN	I
A5	R	E1A	I
A6	R	FR0	I
A7	I	FR1	I
A8	R	FR2	I
A9	R	FR3	R
A10	R	CL1	I
A11	R	CL2	I
A12	R	CL3	I
V3	I	CL4	I
V4	R		
V5	R		
V6	I		
V7	I		
NP	R		
25B	I		
NB2	R		
NB1	R		

I = Installed
R = Removed

FIGURE 25 CONSOLE INTERFACE

The other interface used with GDAS Console is the DLV 11J, four port serial line unit. It is normally used only when a line printer is required, rarely in the field. Channels 1, 2, 3, are normally configured as LPØ, LP1, LP2, respectively, while channel 4 is configured for DEC's default command console; Address 177560, interrupt vector 060.

Complete strapping and configuration must be obtained from the equipment instruction manual.

8.4 ANALOG TO DIGITAL CONVERTER SUBSYSTEM

The Analog to Digital Converter (ADC) used in GDAS is the Preston Scientific GMAD4A. It is a totally self-contained 16 channel Analog to Digital Converter system requiring only a digital interface module for proper operation in the GDAS.

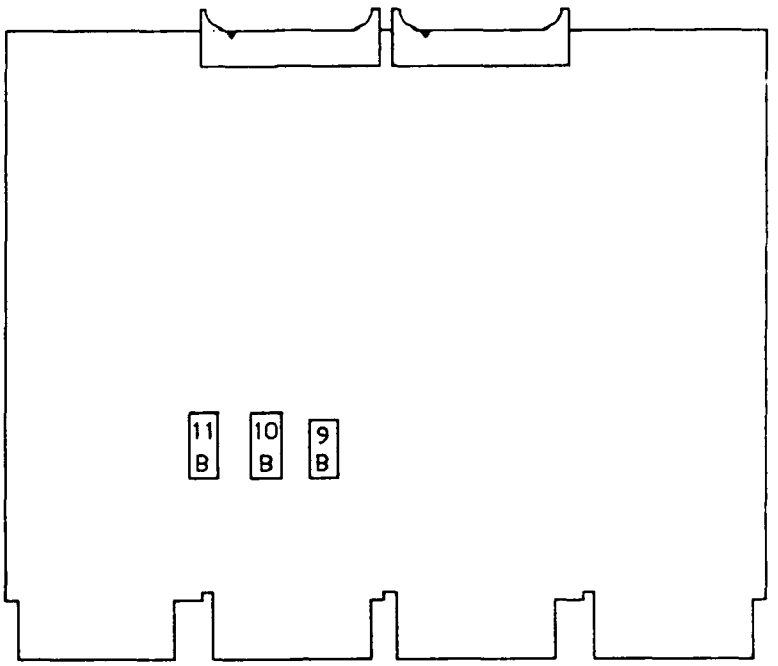
The front end of the Preston is 16 separate high input impedance differential amplifiers, followed by 16 sample and hold circuits and 16 channels of multiplexing. The resultant time sliced signals are fed into one ADC consisting of two 8 bit resolution successive approximation converters. The output of the first converter is compared to the input, and an amplified error signal is produced and fed to the second converter. In essence the second 8 bits is the result of digitization the LSB of the first 8 bits. The results of the two conversions are digitally added for a 15 bit resolution. These conversions are processed through holding circuits for front panel display and output.

The ADC is configured as a 5.25" high unit in a standard 19" rack system, is 19" deep and weighs approximately 40 lbs.

Front panel controls allow for setup, testing, and display, and can be locked out by software control.

8.4.1 ADC DMA INTERFACE

The interface used with this subsystem is an MDB DRV-11B. It is a Direct Memory Access quad height module and is primarily a parallel interface. Device address and interrupt vector location are selectable using board mounted switches 9B, 10B, and 11B. In GDAS these are 772410 and 124 respectively. Figure 26 lists the switch positions for proper address within GDAS.



Pos	SW11B	SW9B	SW10B
1	Closed	Closed	Open
2	Closed	Closed	Closed
3	Closed	Open	Open
4	Closed	Closed	Closed
5	Closed	Open	Closed
6	Open	Closed	Closed
7	Closed	Open	Closed
8	NA	Closed	Open

FIGURE 26 PRESTON PARALLEL INTERFACE

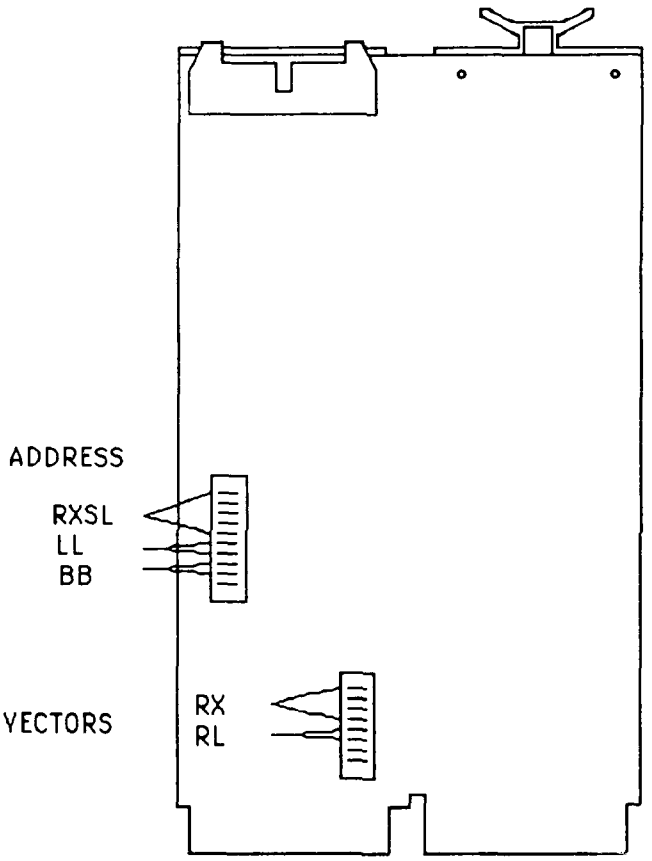
8.5 WINCHESTER/FLOPPY MASS STORAGE DEVICE

The Data Systems Design (now Qualogy Inc.) DSD 880 is a data storage device combining a winchester disk system and a floppy disk system in a single unit. Together with its supplied interface, the unit is totally compatible with all DEC LSI 11 processors. The winchester emulates a high performance disk system, DEC RLO1/RLO2, while the floppy follows DEC RXO2 format. Total storage in the system is 8.8 megabytes (7.8 MB fixed and 1 MB removable). The single interface controller unit is common to both devices, DL and D4, and handles all integration. Existing device handles need not be modified and although the controller can emulate both systems, it cannot do so simultaneously. Each disk drive responds to a different device address, interrupt priority and interrupt vector.

The subsystem is contained in a standard 19" wide rack mountable frame, 5.25" high and 23.75" deep, and its weight is 56.6 lbs. (25.7 kg).

8.5.1 WINCHESTER/FLOPPY INTERFACE

The interface for the DSD 880 is supplied by the manufacturer. It is a dual height card model 8832. To the user its two programming switches are available affecting device addresses, interrupt vectors, bootstrap, and priority. All other jumpers are DSD set up and should not be altered. The jumper configuration for GDAS use is shown in Figure 27. This configuration sets up the DL device (Winchester) as the bootable Resident device.



S1POS	Status	S2POS	Status
0	O	0	S
1	S	1	S
2	O	2	S
3	O	3	S
4	O	4	S
5	S	5	S
6	S	6	S
7	S	7	O
8	S	-	-
9	NA	-	-

S = Short
O = Open

FIGURE 27 DSD880 INTERFACE

8.6 BUBBLE MEMORY

Bubble memory is a complete non-volatile mass storage system that is intended for installation directly into a "Q" bus backplane system. The controller (Bubbl-Control[tm]) is interactive with the "Q" bus and must be installed in the "daisy chain" priority of the bus structure. The memory boards (Bubble-Boards[tm]) do contain jumpers for bus continuity, but require only power from the backplane. Communications or storage is via a 26 conductor ribbon cable, and as a result the Bubble-Boards can be mounted external to the bus if desired.

At present, two types of bubble memory are used in the GDAS. One operates as a "DY" device (double density floppy disk). Bubble-Tec model QBC-11/02 requires a modified DY handler. The other oprates as a "DL" device (fixed disk), Bubble-Tec model QBL 11/02 operating from a standard DL handler. Due to inadequacies in the on board boot procedure (failure to mask the BEVENT interrupt), the boot must be disabled and a full boot installed elsewhere in the system if the ERC clock is used or the device can operate as non resident.

Bubble Boards are removable and transportable without loss of data contained within the magnetic-bubble devices. The primary purpose of bubble memory is in an extreme harsh vibration environment that could destroy the recording heads of DY or DL devices. Also, as the Bubble is completely electronic, there is no rotating media to wear out through long use.

As set up they are strapped for standard device addresses, bootstrap disabled. It is suggested that no charges be made by the user unless full working of the particular handler is understood.

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